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Est. 1988

Statement of Volatility
PN: PCIe-ASCB, PCI-ASCB

Manufacturer Part Number: PCIe-ASCB, PCI-ASCB, includes all types

Manufacturer Part Description:1/2 length PCIe/PCI format design with ASCB function plus PMC position.

Memory Type: FLASH, SRAM, FIFO in ASCB function. PMC module covered by separate document for that device.

Memory Size: Bridge PCIe: Internal registers for configuration, FIFO memory to support link traffic. FIFO on PCIe lanes includes Four, read completion buffers in the uplink direction and one read completion buffer for downlink.
Bridge: PCI – Memory to buffer traffic between the two PCI ports.

Memory Size[FPGAs]: varies with installed FPGA. Xilinx [S3 or S6] for ASCB function.

Volatility: FPGA: SRAM and FIFO memories cleared by power cycle. FLASH is retained through power cycle. FLASH is used to reload FPGA at power-on. Bridge: FIFO memory is continuously rewritten during operation and effectively cleared by this process.

User Accessible: SRAM within FPGA is configured into registers etc. FPGA features are R/W [in many cases] to user software. SRAM contents are lost at power down and re-written with base design from FLASH upon power-on. Bridge: EEPROM can be used to store Bridge configuration values by the user. FIFO within Bridge is not user accessible in the traditional sense as the traffic is flowing through these memories without user control

Clearing Procedure: FPGA: Power cycle or re-write data stored contents per approved procedure. SRAM model for internal and FIFO. Bridge: Use, and Power cycle for FIFO memory.

Notes or Warnings: Installed PMC not covered by this document.