DYNAMIC ENGINEERING
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Est. 1988

Statement of Volatility
PN: PMC-Parallel-TTL

Manufacturer Part Number: PMC-Parallel-TTL, includes all types (-GPIO, etc.)
Manufacturer Part Description: PMC with FPGA and TTL IO, front or rear IO, PLL
Memory Type: FLASH, SRAM
Memory Size: varies with installed FPGA
Volatility: SRAM memories cleared by power cycle. FLASH is retained through power cycle. FLASH is not accessible by user for writing or read-back. FLASH is used to reload FPGA at power-on.
User Accessible: SRAM within FPGA is configured into registers etc. FPGA features are R/W [in many cases] to user software. SRAM contents are lost at power down and re-written with base design from FLASH upon power-on. All data is lost when powered down. When reset, pointers are reset making current data inaccessible.
Clearing Procedure: Power cycle or re-write data stored contents per approved procedure.

Notes or Warnings: None