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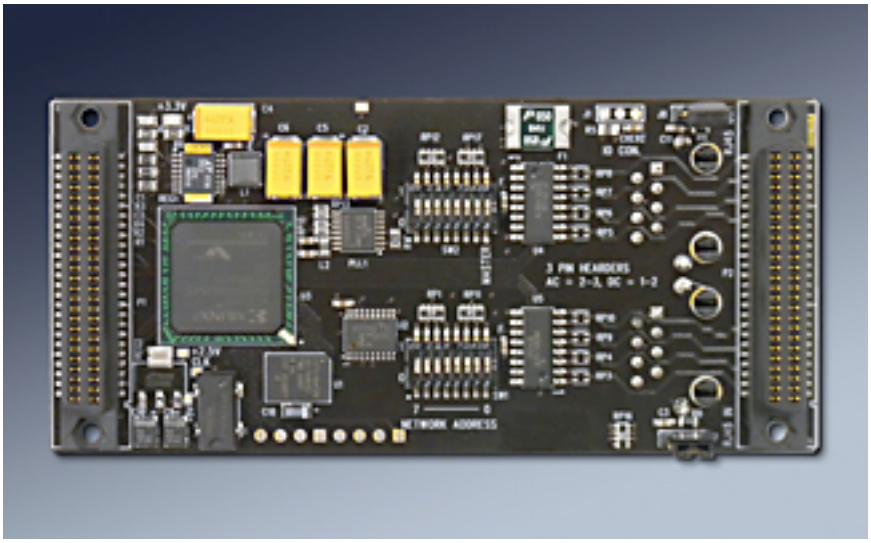
User Manual

IpReflectiveMemory

Reflective Memory Interface
256Kx16
RJ45 or IO connector
IndustryPack® Module



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IpReflectiveMemory
Multi-User Shared Memory Module
IndustryPack® Module

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The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with IP Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Revised September 17, 2015

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Product Description

IpReflectiveMemory is implemented with the idea of offloading the CPU as much as possible. Basically write to store and read to retrieve data from the common image represented by the 256K x 16 array. The memory can be organized in any way that suits the system requirements. In some cases it will be used for message passing and separate segments within the total memory will be defined for each node. In other cases the memory locations will correspond to working data and all nodes will work in the same space.

IpReflectiveMemory is part of the IndustryPack® "IP" Module family of modular I/O components by Dynamic Engineering. IP-ReflectiveMemory provides the ability to share a memory image over a network without CPU overhead or additional HW. Each board has 256K x 16 of SRAM accessed within the IP Memory Space. No set-up is required to use the RAM. When the local memory is updated the address and data are packaged and sent to the next node. The next node will move the update command to its local FIFO for RAM updates and to a second FIFO for Network data. The hardware takes care of all of the data manipulation and checking. The message makes its way around the network until returning to the node of origin where it is deleted.

Start-up is automatic and for most situations the default settings are correct. True plug and play operation. Several options are available to enhance operation for your system.

When powered-on all nodes do a RAM clear and then check if the Master Node. If the Master Node, the Master Status message is transmitted and checked. A timer is used to determine if the Master Status message is "overdue". While checking for Master Status, the Master node will show status with the NetWork activity LED. Other nodes that are properly connected and initialized [RAM loaded] will forward the Status showing the Master Status and Network traffic. Once the Master Status is received at the Master – loop complete – the Master will begin transmitting the Master Enable. When the other nodes receive Master Enable, the nodes are enabled to operate on the network. The other nodes send local status and when received set the local status LED.

During initialization the timer is set to a shorter duration to allow for faster network acquisition. Once the network is established the network checking frequency is reduced to become a low overhead background activity. The initialization rate is 1 mS to allow for 256 nodes each with 1 uS forwarding time. The MasterEnable mode uses a 50 mS time basis to check for changes in network status.

In operational mode the Local Status, Network Traffic, and Master Enable LED's will show activity on the nodes other than Master. The Master will show the local and Network status.

Since the Master Status is shown when it is received the network can be visually checked for the source of an error condition. The Status LED will not be enabled on the node after the issue.

The Master Node keeps internal status to be able to recognize the difference in a restart and a cold start on the network. After a cold start the Master Node will proceed as described above. After a restart the Master will perform a Memory Dump to re-initialize all of the connected reflective memory to match the Master. For example if a network has been operating and the user decides to add another node by disconnecting and splicing in a new node; the network will transition from operational to not operational. It is highly unlikely the user can disconnect and reconnect within the 50 mS between status checks. The Master will be in Status mode until the network is on-line. Once on-line the Master will withhold the Master Enable until the Master Memory is copied to the network. The data is sent back-to-back and takes about 1/4 second to accomplish. Master Enable is transmitted enabling the nodes to operate again. The new node will have a complete copy of the data rather than a cleared memory due to the power on cycle. Software operating on the MasterNode can disable the Node Memory Dump function if automatic reloading is not desired.

The local timer is held in reset when the initial RAM clear is in operation to allow any new nodes or the last to be powered on to hold the network in Status mode until all nodes are fully operational. The memory clear only requires power to be applied and will likely be accomplished long before the local OS is initialized.

Since the Memory and Network operations are executed in parallel there is very little overhead at each node. With the default settings messages are transferred at a rate of 1 per uS between nodes. Since FIFO memory is placed between the receiver and Network the transmitter can work at the same time as the other nodes transmitters to create pipelined operation.

Message traffic is reduced by checking if a new value written to RAM already exists at that location in RAM. If the update is a duplicate the memory location is not transmitted to the network. The IP LED will turn on when you write a new pattern to memory on a card. If the data matches the data in Memory the data is not forwarded and the LED is not flashed. Software on each node can disable the memory matching feature to transmit all writes to RAM. If the RAM Dump – auto reload feature is disabled this can be a good way to reload the data from each node separately.

The design supports communication using 4 twisted pairs. Ethernet wire is the preferred choice with the RJ45 connector model. The IO connector version can use Cat5e wire or similar for the cable and connectors that match the system.

The cable length can be set to “any length” with the caveat that the frequency of operation may need to be adjusted. The base frequency is supplied by a local oscillator set to 18.432 MHz. The initial frequency of network operation is set to the oscillator rate. Software can be used to select the PLL [on board] and change to a user frequency. Cable runs of 200 ft will work with a good quality cable and the default frequency. Shorter distances can operate at higher frequencies. Longer runs may need to operate at reduced rates.

LVDS signaling is used for the IO. Each Input or Output port has 4 twisted pairs. The Input port has 100 ohm terminations. The signals are a reference clock, plus Data, Address, and Control.

D15-D8 of Control is the board address. A pair of 8 position switches are provided to allow the user to select the local address and Master/Target status. The Local address selection is 8 bits allowing for 256 boards in a system with no restrictions on the address chosen. D7-D4 are the type of transaction happening. D3 and D2 are the Master bit and Master Loop Bit. D1 and D0 are the extended address.

The transaction codes are automatically inserted into the message and handled in HW. No user interaction is required. Writing to Memory with new data will cause a Node Update or a Master Update as appropriate. The update will circle the network and be removed by the initiating node. If the message is corrupted the Master node will delete as part of its housekeeping. Status messages are sent by the Master and Nodes to check on the network operation. Error messages can be generated if corrupted messages are received or if a Status message is not received.

D15-D0 for the Data and Address lines are the Data and lower address respectively.

Using 3 signal pairs and a reference means standard cable [Ethernet] and relatively low frequencies create reasonable bandwidth. Each of the signals has a start bit, 16 payload bits, parity, and at least 1 stop / marking state bit. Assuming 2 stop bits between messages the time of flight for a single message is (1 + 16 + 1 + 2) * period. With the default frequency this works out to 1.085 uS. The message traffic between any two nodes can be up to 920 K updates per second. The internal HW operates in parallel and at 2X the clock rate to provide plenty of internal bandwidth.

The PLL can be used to increase the speed of the IO. The LVDS and connector / cable path can handle high speed signals. The architecture of 2X for the internal operation will limit the top end speed. The design is routed with a constraint set to 60 MHz on the 2X clock. IO rates up to 30 MHz can be selected with the PLL when shorter cable runs are used. With the higher speed IO more messages between nodes can be passed per second. In most situations it will be unnecessary to do so. With large networks cutting the delay accumulated across the network may make it useful to do so.

The Internal design is efficient as well with 4 FIFO's strategically placed to allow for bursted data situations – local updates while other nodes are also updating, or IP updates at a rate faster than the Network update rate. The FIFO's are 512 x 48 to store the data, address and other coding requirements.

Status from the FIFO's for Empty, Full, and overflow is available in the status register. The overflow bits are "sticky" and can be cleared by writing back to the status register with the same bits set.

In addition the status register has a bit for the card being enabled to operate on-line – that the Master Enable signal is active – this bit is held once Master Enable is set until Master Status is received. The NodeMatched bit is also in the status register to allow software to select a node to detect messages from. Any external node can be used. Status and Enable messages are filtered out so the status is only set from an update message from the programmed node of interest.

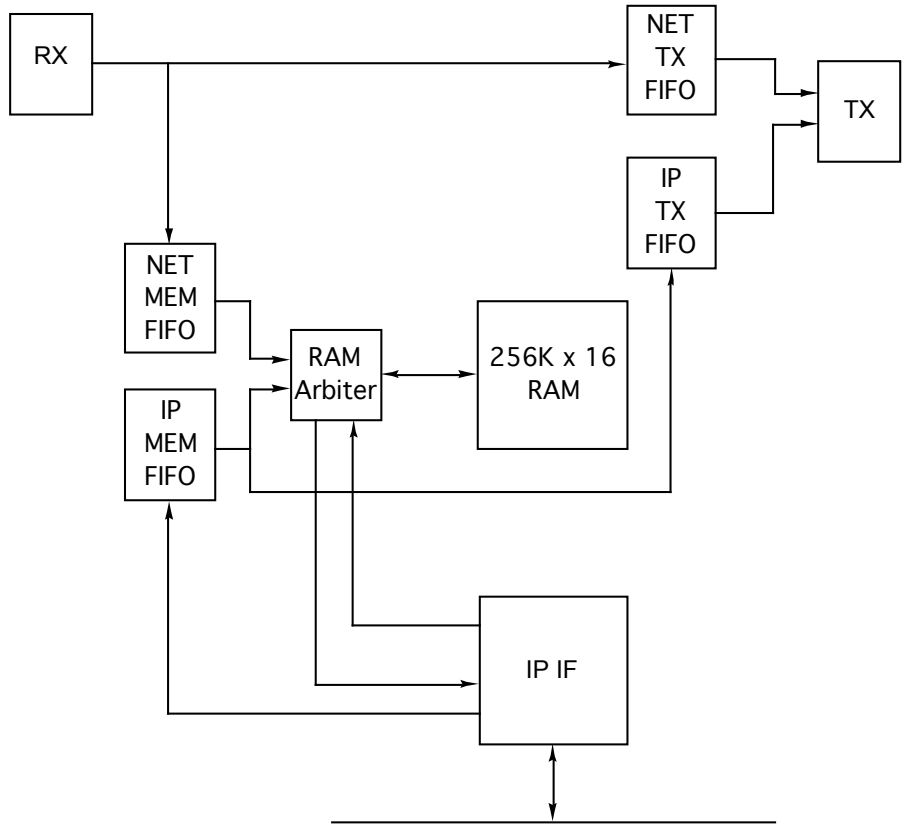

FIGURE 1 IPREFLECTIVEMEMORY DATA FLOW DIAGRAM

The RX Block contains the deserializer, error detection, and packet level control. Same node messages are deleted, status messages are passed through without updating the RAM, Updates are forwarded to the RAM.

If the Master node, The RX section also tests the message for the loop bit and if set the message is removed. In addition the Master or local Status message is generated and timed to make sure the network is fully functional.

The TX Block arbitrates between the network messages and local updates via the IP bus interface. The data is serialized and shipped out. All TX timing is controlled here.

The RAM and internal data traffic is run at 2x the TX IO rate. The RX side uses the received clock to de-serialize and move to the first level of register holding. The enable signal used to load the register is cross-clocked to change domains to the reference rate used for the transmitter. The transmitter uses an internal [always available] clock. By changing domains to an “always on” clock the receive state-machine can operate when the link is down [disconnected or the node upstream is off] and recover from various situations. It does mean that the reference rate for the TX on each node should be similar to allow the nodes to communicate properly. The default settings take care of this. Using a common setting across the network with the PLL also will take care of this requirement.

The Tx side operates at the programmed rate [default = 18.432 MHz]. The IP port operates at the IP slot rate. The IP interface is 8 and 32 MHz compatible. When operating at 32 MHz the hardware interface is faster.

The IP Port has a write through FIFO that captures the Address and Data from the host and responds immediately allowing the IP bus to be released. The RAM arbitration unit checks the status of the Network MEM FIFO and the IP MEM FIFO to determine if there is data to move to RAM. From the network side a simple direct access write will take place. From the IP side a read is first performed, and the data read compared to the FIFO contents. If the data matches no write is required, and the transaction is complete. If the data does not match, the local RAM is updated and the data/address are packaged with the local address etc and moved to the IP TX FIFO.

For a read from the local RAM the IP interface requests an access from the RAM Arbitration unit. The Arbitration Unit reads the location and moves the data to a register. The Arbitration unit acknowledges the request to the IP interface allowing completion of the read.

Since IP accesses are asynchronous to the RAM and IO clock rates; meta-stable protection is employed. Since the IP side is waiting for the acknowledge, using a higher rate clock [32 MHz] will result in faster accesses – faster processing on the handshake signals and faster reaction once the response is detected.

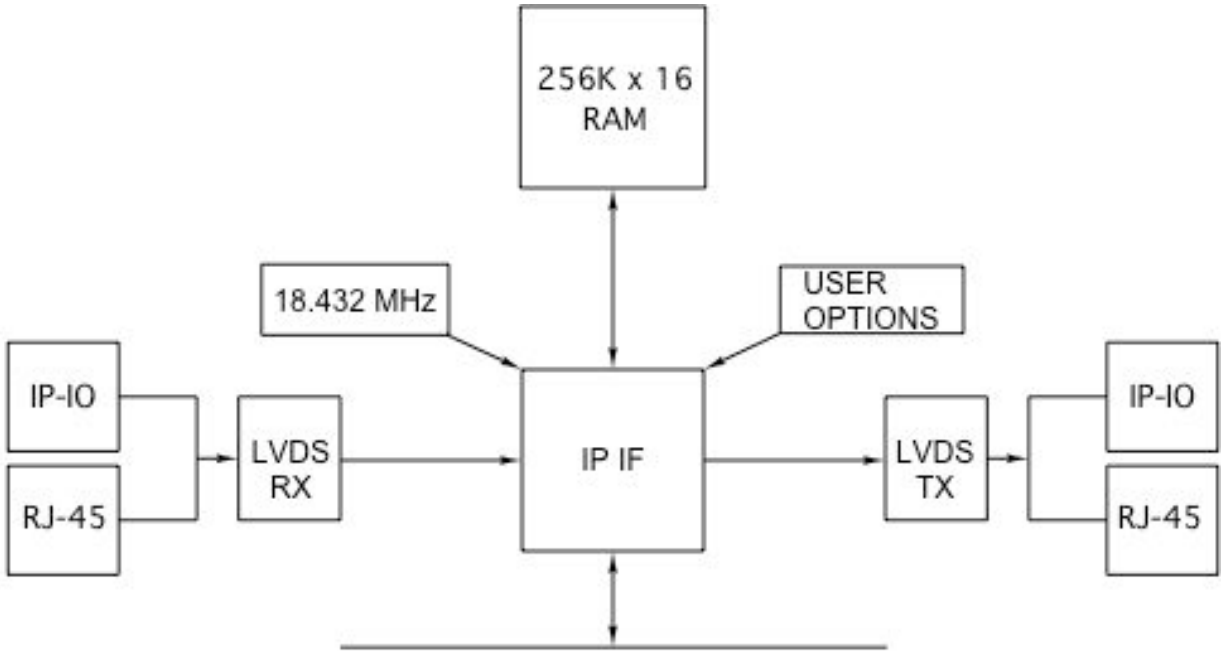

FIGURE 2 IPREFLECTIVEMEMORY BLOCK DIAGRAM

The receive and transmit sides can be supported with either RJ-45 or IO connector based cabling. The RJ-45 connectors are mounted on the rear of the board with the cable side oriented toward the IO connector. The height of the RJ-45 connectors makes this configuration a Type III IP Module and will likely require an extra slot in your system. The IO connector option uses the IP Module IO connector instead of the RJ-45 connectors. The IO connector configuration is a Type II with only low profile components on the rear.

The RJ-45 option has the advantage of not relying on the carrier interconnection to the Carrier connector. The IO connector has the advantage of lower profile. The pinouts for the IO connector were chosen to run on likely IO connector pairs and in many cases somewhat differential routing.

The routing of the LVDS signals on the IP-ReflectiveMemory card are controlled impedance, matched length differential pairs. The connectors are isolated with two sets of 0 Ω resistor jumpers. The resistors are on opposite sides of the board with a single via connecting the resistors to the RX/TX LVDS interface. The stub length is essentially 0 in one case and 1/16th in. in the other and matched length in both.

Currently the User Options include the node address and Master/Target board operation. Two surface mount “dipswitches” are used to make the selections. One switch is dedicated to the Node address. The bits are labeled 7-0 and the sense is labeled 1-0 for the Network Address. Each board in the system must have a unique address for proper operation.

The second switch set controls the Master [or not] status. Moving the switch toward the “Master” indication in the silk screen will select the master mode. There must be one and only one master on the network. The network address is independent of the master selection.

Hardware is supplied with the address set to “00” and the options cleared.

LED’s are supplied for several functions. On the component side a 3.3V LED is shown to indicate the switching power supply is functional. On the rear are 8 LED’s with labels: Master Status, Master Enable, Error Detected, Local Status, IP [access] and Network[Access]. There are two additional unlabeled LED’s for future expansion. The LED’s have a control register to select a Forced Flash or direct access modes. The default is Forced Flash. When an event occurs the LED is enabled for 1/4 second and then disabled for 1/4 second before “looking” for the next trigger. In the direct access mode the trigger causes a 1/4 second on time for the LED and if a second trigger comes prior to the 1/4 second completing the counter is reset. A string of pulses closer than 1/4 second has the effect of always on.

The LED action can be observed when the RAM tests included in the UserAp software is run. The UserAp software is included with the IpRelectiveMemory Driver package. The tests load the RAM on one card and check that the other cards are updated. The two spare LED’s are programmed to show the board being updated and the one being checked in each test. The LED’s are programmed to be activity based for the board with the direct update and forced flash mode for the board being updated by the network.

Headers with low profile shunts are provided to allow the user to select the termination for the shield or reference for the IO connector signaling. The Shield can be AC/DC or open connected to ground. The silk has a note with the definitions for the shunts. The IN and OUT Shields are handled separately.

IpReflectiveMemory conforms to the IndustryPack® standard. This guarantees compatibility with compliant carrier boards. Because the IpReflectiveMemory may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Carrier board, with final system implementation on a different one. For example the PCI3IP – PCI carrier for IP Modules can be used for development in a conventional PC. Later the hardware and software can be ported to the target. http://www.dyneng.com/pci_3_ip.html

With the Dynamic Engineering Windows driver collection for IP and carrier modules a Parent – Child architecture is employed. The IP portion of the driver is directly portable between the various Dynamic Engineering IP carriers [PCIe3IP, PCI3IP, PCIe5IP, PCI5IP, PC104pIP, PC104p4IP, cPCI2IP, cPCI4IP etc]. The parent portion of the driver contains the carrier specific design information. This means that software developed for the IpReflectiveMemory on one platform can be directly ported to another. PCI to cPCI for example.

Designers can make use of the Dynamic Engineering carrier driver for non-Dynamic Engineering IP modules using the Generic IP capability built into the parent portion of the driver. IP modules that the carrier driver does not recognize are installed as "generic" and accessed with a address, data interface model. Software developed for the Generic mode can also be ported between modules.

IpReflectiveMemory is tested with a combination of internal and external tests. The registers can be tested with R/W tests, the Network can be tested with a series of inter-board loop tests. Three boards are used to test each board in initiator, pass through and read-back target.

Interrupts are supported by IpReflectiveMemory. A force interrupt for software development and test is provided plus an interrupt from matching the address from a node in the system. The address is programmable, and the interrupt is SW controlled. Status is provided separate from the interrupt to allow the NodeMatch capability to be used in a polled mode as well.

Address Maps

Address Map Internal

IPREFMEM_BASE	0x0000 //0 Base control register
IPREFMEM_VECTOR	0x0002 //1 Interrupt vector register
IPREFMEM_INT_STATUS	0x0004 //2 Interrupt status read
IPREFMEM_NODESWITCH	0x0006 //3 Node Address, Node Options read only
IPREFMEM_MESSAGECOUNT	0x0008 //4 Message Count, read only
IPREFMEM_ADDRESSMATCH	0x000A //5 Address Match
IPREFMEM_INFO	0x000C //6 Address where carrier info is stored
IPREFMEM_LED_CNTL	0x000E //7 LED Forced Flash selection register
IPREFMEM_ERRORCOUNT	0x0010 //8 Error Count Read, Clear Write

FIGURE 3 IPREFLECTIVEMEMORY INTERNAL ADDRESS MAP

IpReflectiveMemory relative addresses
RAM is on word boundaries in **Memory Space**
256K x 16 is total RAM size
Offsets 0 – 3FFFE

Programming

Programming IpReflectiveMemory requires only the ability to read and write data from the host. The base address refers to the first user address for the slot in which the IP is installed.

Depending on the software environment it may be necessary to set-up the system software with IpReflectiveMemory "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware. Other OS may be more “plug and play”. The Dynamic Engineering Driver operates in a “plug and play” mode using parent ⇔ child architecture.

The hardware is self starting. When powered up the master node will establish the network and then enable the rest of the nodes. The local memory will automatically be kept in synchronization with the other memories in the system. In order to access the local memory the Memory space for the slot the IP-ReflectiveMemory is installed into is used. Writing automatically updates the other nodes in the system. Reading returns the value in the local memory.

If the special functions are used, access to the IO space is utilized. The bit maps for the IO space registers follows in the next section.

Interrupts are available to alert the local host when a specific node has made a memory update.

The Dynamic Engineering IpReflectiveMemory driver for Windows 2000 and XP manages the interaction and can set-up the transfer for you. The driver is easily integrated into a Visual studio programming environment. Please refer to the driver manual for more information.

Register Definitions

IPREFMEM_BASE

IPREFMEM_BASE 0x0000 // 0 base control register offset

BASE Control Register

DATA BIT	DESCRIPTION
15	PLL_SDAT
14	PLL_S2
13	PLL_SCLK
12	PLL_EN
11	NetIdDisable
10	NetPtDisable
9	NetIpDisable
8	NetRamDisable
7	RamDumpDisable
6	ForceWrite
5	spare
4	NodeMatchIntEn
3	Spare
2	ClkOutSel
1	RamClkSel
0	INTFORCE

FIGURE 4 IPREFLECTIVEMEMORY BASE CONTROL REGISTER BIT MAP

Reset is affected by the switch position of the options switch #1. [next to the “master” switch] When set to ‘0’ all bits are reset to “0000”. When set to ‘1’ the register resets to “00C0” with the effect of having the default condition for ForceWrite and RamDumpDisable = ‘1’. *For the VR1 version only* the ForceWrite and RamDumpDisable are read only bits in this register with their value set by the position of the switch.

Intforce: when set causes an interrupt to be generated to the system. Useful for debugging and software test.

RamClkSel : when '0' select 2x osc clock when '1' select PLLA for the RAM clock reference. If set to select the PLLA output be sure to have the PLLA programmed to the desired frequency prior to switching. PLLA should be set to 2X the output rate or more

ClkOutSel: when '0' select 1x osc clock when '1' select PLLB for the TX IO rate. If set to select the PLLB output be sure to have the PLLB programmed to the desired

frequency prior to switching. PLLB should be set to 1/2 of the RAM clock rate or less.

NodeMatchIntEn: set to 1 for NodeMatch Interrupt Enable to be enabled. Cause an interrupt when a received RAM update message matches the programmed AddressMatch register. Clear the interrupt by writing back to the status register. Clearing this bit will disable the interrupt and not clear the source.

ForceWrite: set to 1 for ForceWrite mode where all writes to local RAM are sent to the network. Set to 0 for standard operation where all writes to local RAM are checked against local RAM and only changes in data are sent to the network.

RamDumpDisable: set to 1 to Disable automatic RAM Dump operation. Affects master mode nodes only. Set to '0' to enable RAM Dump operation. RAM Dump transmits the contents of the Master Node local RAM when the network has transitioned from operational to "down" and back to operational.

NetSramDisable: when '1' the RAM is not updated from the network. The local copy of memory is isolated from updates from the network. Please note that this does not stop the network message forward capability. This bit also does not stop updates to the local memory from being written to the network. Basically a protected copy on the network. Leave set to '0' for normal operation.

NetIpDisable: when '1' the Network is not updated from a RAM write via the Host IP interface. The local copy of memory can be updated without the network knowing about it. Leave set to '0' for normal operation.

When NetIpDisable is set along with NetSramDisable the local RAM is effectively isolated from the network. The network is still functional in a pass through configuration.

NetPtDisable: when '1' the Network is not updated from a received message => used to cause Pass Through errors. This bit is for error testing only. Since Network messages are not passed through the MasterEnable will no longer be passed and a timeout will occur at the master causing a change to Master Status. Leave set to '0' for normal operation.

NetIdDisable: when '1' the received message is not checked for the local address => used to cause an error at the master for trip bit already set. Leave set to '0' for normal operation.

PLL IF programming.
The PLL reference frequency is 18.432 MHz. The PLL is a Cypress 22393. The PLL is programmed with the output file generated by the Cypress PLL programming tool. [CY3672 R3.01 Programming Kit or CyberClocks R3.20.00 or later.]

The .JED file is used by the Dynamic Driver to program the PLL. Programming the PLL is fairly involved and beyond the scope of this manual. For clients writing their own drivers it is suggested to get the Engineering Kit for this board including software, and to use the translation and programming files ported to your environment. This procedure will save you a lot of time. The output file from the Cypress tool can be passed directly to the Dynamic Driver [Linux or Windows] and used to program the PLL.

pll_en : Software output enable control for PLL
pll_sclk: Output to pll command clock
pll_s2 : PLL S2/Suspend
pll_sdat : When PLL_EN is set the output follows the register bit otherwise held in tristate. When read the state of the IO pin is returned.

IPREFMEM_VECTOR

IPREFMEM_Vector 0x0002 // 1 IP vector port

Vector Port

DATA BIT	DESCRIPTION
15-8	Spare
7-0	vector

FIGURE 5 IPREFLECTIVEMEMORY VECTOR BIT MAP

If the system uses a vectored interrupt approach then the vector port should be initialized to the vector value assigned to this device. IpReflectiveMemory can be used as vectored or auto-vectored. In auto-vectored situations this port is unused. The Status port can be used to determine the source of any pending interrupts from IpReflectiveMemory.

Default is 0xFF for data.

IPREFMEM_INT_STATUS

IPREFMEM_INT_STATUS 0x0004 // 2 base Status register

Status Register

DATA BIT	DESCRIPTION
15	NET_TX_FIFO_OVFL
14	NET_MEM_FIFO_OVFL
13	IP_TX_FIFO_OVFL
12	IP_MEM_FIFO_OVFL
11	NET_TX_DATA_FULL
10	NET_MEM_FIFO_FULL
9	IP_TX_DATA_FULL
8	IP_MEM_FIFO_FULL
7	NET_TX_DATA_MT
6	NET_MEM_FIFO_MT
5	IP_TX_DATA_MT
4	IP_MEM_FIFO_MT
3	RAM_BUSY
2	NODE_ENABLED
1	NODE_MATCH_LAT
0	INTSTAT_INT_REQ0

FIGURE 6 IPREFLECTIVEMEMORY INTERRUPT STATUS BIT MAP

INTSTAT_INT_REQ0: is set when INTFORCE, or NODE_MATCH_LAT are set and the corresponding mask is enabled. This bit is cleared by dealing with the interrupt source.

NODE_MATCH_LAT is set when an update message is received from the node programmed in the AddressMatch register. After changing the defined address this bit should be cleared. The bit is a “sticky” bit meaning that the status is retained until the bit has been explicitly cleared by writing to the status register with this location set. If the corresponding interrupt is enabled, the interrupt is cleared by clearing this bit.

NODE_ENABLED is a status bit indicating that the node has received MasterEnable and has not received MasterStatus. The MasterEnable and MasterStatus messages are transitory in nature. The NODE_ENABLED signal is set when MasterEnable is received and cleared when power up or MasterStatus is received.

RAM_BUSY: is set during initialization while the RAM is being cleared. The IP holding FIFO is still available, and care must be taken not to overrun the FIFO as no data will be read out until the clear is complete. Normally the OS will take much longer to start-up than it takes for the RAM to clear. If you have an instant on system checking this bit

before use is recommended. The Network side is automatically held off until the RAM clear is complete on all nodes.

IP_MEM_FIFO_MT when set indicates the holding FIFO between the IP interface and the RAM is empty.

IP_TX_DATA_MT when set indicates the holding FIFO between the IP interface and the transmitter is empty.

NET_MEM_FIFO_MT when set indicates the holding FIFO between the network interface and the RAM is empty.

NET_TX_DATA_MT when set indicates the holding FIFO between the network receiver and the transmitter is empty.

IP_MEM_FIFO_FULL when set indicates the holding FIFO between the IP interface and the RAM is full.

IP_TX_DATA_FULL when set indicates the holding FIFO between the IP interface and the transmitter is full.

NET_MEM_FIFO_FULL when set indicates the holding FIFO between the network interface and the RAM is full.

NET_TX_DATA_FULL when set indicates the holding FIFO between the network receiver and the transmitter is full.

The OverFlow bits if used should be cleared first then read later to insure new events are being observed. It is suggested that the bits are checked as part of a status loop - if one exists in your system. The bits should never be set, and if they are corrective action should be taken. Usually the cause of the overflow will be due to user clock changes or operating above the link rate. Most systems for IP Modules do not have DMA capability, and most can't sustain rates above the link rate.

IP_MEM_FIFO_OVFL when set indicates the holding FIFO between the IP interface and the RAM was full when a write occurred. This is a sticky bit and must be cleared by writing back to the status port with this bit set. When set this indicates that at least one update to the local RAM did not make it to the local RAM. Most likely occurrence would be writing to the RAM during initialization. The RAM update rate is relatively fast compared to system write speeds.

IP_TX_FIFO_OVFL when set indicates the holding FIFO between the IP interface and the transmitter was full when a write occurred. This is a sticky bit and must be cleared

by writing back to the status port with this bit set. When set this indicates that at least one update to the local RAM did not make it to the Network. If the RAM update rate is higher than the network rate for an extended period this error can occur. The FIFO is 512 deep. The Arbiter within the TX logic will alternate between the Network and IP FIFO's if both have data to send. The minimum bandwidth available to each node would be almost 500 K updates per second. More if other nodes are not updating at the same time. Alternatively if the TX frequency is reduced to accommodate longer cables and the system rate has not changed the FIFO's can back up.

NET_MEM_FIFO_OVFL when set indicates the holding FIFO between the network interface and the RAM was full when a write occurred. This is a sticky bit and must be cleared by writing back to the status port with this bit set. When set this indicates that at least one update from the network did not make it to the local RAM. The RAM is three ported. It would take a combination of continuous reads and writes from the IP port to reduce the access to the RAM enough to effect the Network update capability. Alternatively if the user selected clocks are not set to provide enough margin to the RAM clock compared to the Input clock rate overflow can occur.

NET_TX_FIFO_OVFL when set indicates the holding FIFO between the network receiver and the transmitter was full when a write occurred. This is a sticky bit and must be cleared by writing back to the status port with this bit set. For this FIFO to fill up the TX rate would need to be lower than the RX rate and enough traffic received for the data to pile up on the NetWork side. In addition if the local RAM is written to a lot with new data so that the IP side is using half of the available bandwidth this situation can happen sooner. If your system is using PLL clocks and this bit is set try increasing the TX port to more closely match the upstream port or decrease all ports to match.

IPREFMEM_NODESWITCH

IPREFMEM_NODESWITCH 0x0006 // 3

Node Address and Options Register

DATA BIT	DESCRIPTION
15-8	Node Options
7-0	Node Address

FIGURE 7 IPREFLECTIVEMEMORY NODESWITCH BIT MAP

The Node Address is the address set on the Network Address switch mounted to the PCB. The address read through this port will be used to identify messages from this node on the network.

Node Options:
Bit 0 switch, Bit 8 in register: Master Bit. When this switch is set to the Master position – indicated in the silk screen, this board becomes the master for the network. Each network is required to have one master enabled node. When the switch it pointed away from the master position the node is a target.

VR1 Specific Options:
Bit 1 switch, bit 9 in register: Affects the default reset options in the base control register [IPREFMEM_BASE].

Bit 7 switch, Bit 15 register: Selects the reset state for the RAM. Setting the switch [same position as Master] causes the SRAM to be initialized to 0x8000. The default initializes to 0x0000.

IPREFMEM_MESSAGECOUNT

IPREFMEM_MESSAGECOUNT 0x0008 // 4

Message Count Register

DATA BIT	DESCRIPTION
15-0	Message Count

FIGURE 8 IPREFLECTIVEMEMORY MESSAGE COUNT BIT MAP

The message count register can be read to see how many valid network messages of all kinds have been received by the card. Since status messages are counted there will be at least 1 message per node per 50 mS [status message time]. The count initializes to x“0000” and counts through 0x”FFFF” before rolling over.

IPREFMEM_ADDRESSMATCH

IPREFMEM_ADDRESSMATCH 0x000A // 5

Message Count Register

DATA BIT	DESCRIPTION
15-8	Spare
7-0	NodeAddressMatch

FIGURE 9 IPREFLECTIVEMEMORY ADDRESSMATCH BIT MAP

The address to match in the receiver is stored in this register. The lower byte will be matched against all received valid update messages. When the message address matches the NodeAddressMatch register the NodeMatch status bit is set. When the address is changed the status bit should be cleared.

IPREFMEM_INFO

IPREFMEM_INFO 0x000C // 6

Location Register

DATA BIT	DESCRIPTION
15-11	spare
10-3	Carrier Switch
2-0	Carrier Slot

FIGURE 10 IPREFLECTIVEMEMORY ADDRESSMATCH BIT MAP

The location register is updated by the carrier driver during initialization. The IP-ReflectiveMemory Driver can access this information later to determine the carrier and location on the carrier that this node is installed into. Once the IP-ReflectiveMemory Driver is started the user software can use this as a general purpose register. The IP Driver stores a local copy in RAM to allow the user software to determine which node it is talking to when multiple nodes are present in a PCI based system with dynamic addressing. Please note that this function is supported on all Dynamic Engineering carriers and may not be supported on other products.

In a Windows system the user software will query for the installed devices and the devices will be returned in order. The issue is that the order can change and there is no way to directly tell with software which card you are controlling at the moment. The node address could be used in this boards case, but to be consistent with our other products we are using the INFO register method to provide a method of matching up devices with locations. The user software can retrieve the devices present and then match them up to the physical hardware based on the carrier switch setting and slot on the carrier. In some systems knowing which board is controlling which machine can be important. Please see the software manual and userap reference software for examples of working with multiple cards. The userap software prints out the device number and associated slot and switch settings. Your software can use the information without printing out for proper access control.

This is only important if you have multiple cards visible to the same CPU.

IPREFMEM_LED_CNTL

IPREFMEM_LED_CNTL 0x000E // 7 base control register offset

BASE Control Register

DATA BIT	DESCRIPTION
15-8	Spare control bits
7	Spare LED 1
6	Spare LED 0
5	LedNetMsgSentFlEn
4	LedIpMsgSentFlEn
3	LedLocalStFlEn
2	LedErrorFlEn
1	LedMasterEnFlEn
0	LedMasterStFlEn

FIGURE 11 IPREFLECTIVEMEMORYLED CONTROL REGISTER BIT MAP

The Led XXX Fl En signal bits are the Flash Enables for the associated bits. When set the LED will trigger and retrigger from each event detected. Each re-trigger event will reset the count to 0x000 to provide the full 1/4 second on time from the last trigger event. When cleared ('0') the LED will trigger from the first event, count for 1/4 second with the LED on, count for 1/4 second with the LED off, then retrigger. This is the Forced Flash mode. The effect is to filter out the trigger events between the first on and the next one after the 1/2 delay.

The Basic network operational LED's will flash continuously since the base rate for the status checks is less than <<1/2 second [50 mS]. Other activity LED's will depend on user activity – mainly the IP activity LED.

Please note that activity from one node becomes Network activity for the other nodes.
Control Bit definitions:
LedMasterStFlEn = LED for Master Status
LedMasterEnFlEn = LED for Master Enable
LedErrorFlEn = LED for Errors detected
LedLocalStFlEn = LED for Local Status
LedIpMsgSentStFlEn = LED for Local Node sent a message [data or RAM dump]
LedNetMsgSentStFlEn = LED for Network Traffic forwarded – can be status [any node] or data from other nodes.

Spare LED 0 and Spare LED 1 when set cause the corresponding LED's on the rear of

the board to be illuminated. When cleared the LED's are off. Spare LED 0 is closest to the NETWORK LED. The LED's are available for any user purpose.

IPREFMEM_ERRORCOUNT

IPREFMEM_ERRORCOUNT 0x0010 // 8

Message Count Register

DATA BIT	DESCRIPTION
15-0	Error Count

FIGURE 12 IPREFLECTIVEMEMORY ERROR COUNT BIT MAP

The error count register can be read to see how many invalid network messages of all kinds have been received by the node. The count initializes to x"0000" and counts through 0x"FFFF" before rolling over. The count can be zero'd by writing any pattern to the same register. In Master Mode under certain conditions the MasterStatus message can cause errors to be counted during initialization. Nodes changing state during the transmission of a message or large electrical interference situations are the most likely causes of errors.

Please note that the Master node filters out errors when acquiring the network in the initial phase of initialization. Once the network is passing a message the error checking will set [or not] the error bit as required. The LED for error's will flash and the counter will advance when errors are detected during normal operation.

Interrupts

IpReflectiveMemory interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with an IpReflectiveMemory interrupt the software must read the status register(s) to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

The interrupt is mapped to INT0 on the IP connector, which is mapped to a system interrupt via the host [carrier] device. The source of the interrupt is obtained by reading the Interrupt Status register. The status remains valid until that bit in the status register is cleared.

When an interrupt occurs, the Master channel interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the status and enable the channel interrupt again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the Interrupt Status register.

Loop-back

The Engineering kit has reference software, which includes an external loop-back test. The test requires an external cable. We used Cat5E Ethernet cable to interconnect the output port of one device to the input port of the next device. The software has explicit tests for 3 devices and can easily handle 5 based on the initialization in “main.c” More devices can be handled by expanding the initialization loop.

The loop must be complete. The last device output needs to be connected back to the first device input.

One master per network.

Unique address per node.

Max of 256 nodes per network.

A network of 1 should have the output connected back to the same board input.

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The location of the ID PROM in the host's address space is dependent on which carrier is used.

Standard data in the ID PROM on the IpReflectiveMemory is shown in the figure below. The values where different for the VR1 version are shown after the "/" For more information on IP ID PROM's refer to the IP Module Logic Interface Specification.

Address	Data	
01	ASCII "I"	($49)
03	ASCII "P"	($50)
05	ASCII "A"	($41)
07	ASCII "H"	($48)
09	Manufacturer ID	($1E)
0B	Model Number	($0C) IpReflectiveMemory
0D	Revision	($B5/$C1)
0F	reserved	($00/$01) Customer Number
11	Driver ID, low byte	($00) Design Number
13	Driver ID, high byte	($00)
15	No of extra bytes used	($0C)
17	CRC	($04/$68)

FIGURE 13 IPREFLECTIVEMEMORY ID PROM

IpReflectiveMemory Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the IpReflectiveMemory. Pins marked n/c below are defined by the specification, but not used on the IpReflectiveMemory. Also see the User Manual for your carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSEL*	4	29
D1	n/c	5	30
D2	MEMSEL*	6	31
D3	n/c	7	32
D4	INTSEL*	8	33
D5	n/c	9	34
D6	IOSEL*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	INTREG0*	17	42
D14	A4	18	43
D15	n/c	19	44
BS0*	A5	20	45
BS1*	n/c	21	46
n/c	A6	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

NOTE 1: The no-connect signals above are defined by the IP Module Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IP Module.

FIGURE 14 IPREFLECTIVEMEMORY LOGIC INTERFACE

IpReflectiveMemory IO Pin Assignment

The figure below gives the pin assignments for the IP Module IO Interface on the IpReflectiveMemory if the IO option is selected. Also see the User Manual for your carrier board for more information. JTAG used to program FPGA FLASH.

3.3V	DATAIN0N	1	26
GND	DATAIN0P	2	27
	DATAIN1P	3	28
TDI	DATAIN1N	4	29
TMS	DATAIN2N	5	30
TCK	DATAIN2P	6	31
TDO	CLKINP	7	32
	CLKINN	8	33
	GND*	9	34
	GND*	10	35
	GND*	11	36
	GND*	12	37
	GND*	13	38
	GND*	14	39
	GND*	15	40
	GND*	16	41
	DATAOUT0N	17	42
	DATAOUT0P	18	43
	DATAOUT1P	19	44
	DATAOUT1N	20	45
	DATAOUT2N	21	46
	DATAOUT2P	22	47
	CLKOUTP	23	48
	CLKOUTN	24	49
		25	50

NOTE: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the IP Module.

FIGURE 15 IPREFLECTIVEMEMORY IO CONNECTOR PINOUT

GND* = AC / DC/Open based on J1 header shunt setting.

IpReflectiveMemory RJ45 Pin Assignment

The figure below gives the pin assignments for the IP Module RJ45 pin assignments for boards with the RJ45 option.

Connector Pin	DESCRIPTION
8	DATA0N
7	DATA0P
6	DATA2N
5	DATA1P
4	DATA1N
3	DATA2P
2	CLKP
1	CLKN
Shield	J7,J8 shunts for AC/DC/Open shields

FIGURE 16 IPREFLECTIVEMEMORY RJ45 PINOUT

J2 is the Input and J3 is the Output RJ45 connector. Both are marked with the reference designator and INPUT or OUTPUT. Both have the same relative pinout to allow for a standard Ethernet cable to be used for interconnection. The pinout is a result of the cable decision.

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions were chosen with noise immunity and cable compatibility in mind. The pairs should be connected with standard CAT5E or better wiring for best results.

Cable hints. The cable will have a lock to retain the cable in the RJ45 connector. It is important to keep the tab intact. Since the clearance to the tab is small it can sometimes be difficult to remove the cable after being assembled. A small flat blade screwdriver can be used to “deactivate” the tab without damaging the cable.
In addition of your cable has a hood over the tab, and you plan to remove and insert the cable multiple times; it is a good idea to remove the hood.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the LVDS devices rated voltages.

For extreme situations [electrically] where multiple large motors are starting / stopping etc. induced currents within the cable can cause errors to be detected. The network will automatically re-establish itself and synchronize the memory to match the master node. This is similar to the case where the network is disconnected either physically or by a machine being powered down.

If induced noise is causing errors, please check the cabling and make sure the shields are properly tied to ground on one side. It may be necessary to go to higher grade cable. Please note that the shield ground on the card is tied to both the RJ connector shield and the IO connector shield. In some cases the IO connector ground may be easier to use than the RJ45 shield ground.

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. IpReflectiveMemory is constructed out of 0.062 inch thick high temp ROHS compliant FR4 material.

Options are available for ROHS and standard processing of the SRAM based versions with either connector type. The FRAM option is only available with ROHS processing.

Through hole and surface mounting of components are used.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IP Module provides a low temperature coefficient of .89 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the IP. The coefficient means that if .89 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The IpReflectiveMemory design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $125. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
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Specifications

Host Interface:	IP Module 8 and 32 MHz capable
Network Interface:	4 LVDS signals, Input and Output ports
Tx Data rates generated:	Programmable. 18.432 MHz default with PLL support
Software Interface:	Control Registers, Status Ports
Initialization:	Hardware Reset forces all registers [except vector] to 0. RAM is auto-initialized, Network auto configures
Access Modes:	IO, Memory, ID, INT spaces (see memory map)
Wait States:	minimized based on programmed clock rate. Write through CACHE to RAM
Interrupt:	Programmable Node Interrupt. Wait on update message from a specific node.
Onboard Options:	Most Options are Software Programmable. Switch options for Network Address and Master/Node operation
Interface Options:	Two RJ-45 connectors or IP IO connector routed through IP Carrier. Cat5E or better cable recommended. Ethernet compatible with RJ-45 option.
Dimensions:	Type II/ with IO option and type III with RJ-45 option.
Construction:	High temp ROHS compatible FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.
Temperature Coefficient:	.89 W/^{o}C for uniform heat across IP
Power:	Typical **180** mA @ 5V typical with idle traffic on network.
Temperature Range	Commercial and Industrial options. 0C⇔70C and –40C⇔85C respectively. Conformal Coating option for condensing environments

Order Information

IpReflectiveMemory	IP Module with ReflectiveMemory 256Kx16 implementing Network using RJ45 connectors. ROHS processing is standard with this design.
-IO	Use IP IO connector instead of the RJ-45 connectors.
-CC	Conformal Coating option
-ET	Extended temperature option => upgrade to industrial temperature parts [-40c ⇔ +85c or better]
Eng Kit–IpReflectiveMemory	IP-Debug-IO - IO connector breakout IP-Debug-Bus - IP Bus interface extender IpReflectiveMemory Driver and reference software Technical Documentation, 1. IpReflectiveMemory Schematic Data sheet reprints are available from the manufacturer's web site reference software.

***Note**: The Engineering Kit is strongly recommended for first time* IpReflectiveMemory *purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not guaranteed to be current or complete manufacturing data, nor is it part of the product specification.