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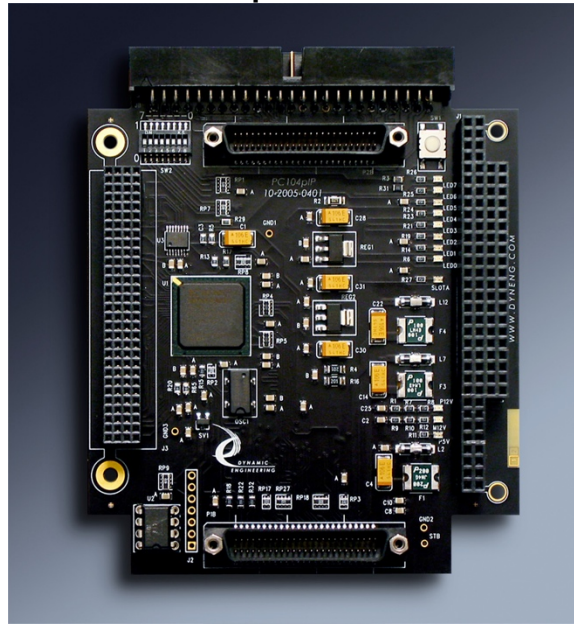http://www.dyneng.com
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Est. 1988

PC104pIP
User Manual
Integrated PC/104p ⇔ IP Module Carrier

Key Features
Fast Access with integrated PCI ⇔ IP Bridge
8/32 MHz IP operation
8/16/32 bit accesses supported
Data Alignment – Byte and Word Swapping
Watch Dog Timer
LEDs - Power, IP Access, User
Multi-board support

M a n u a l   R e v i s i o n   0 1 P 2
Fab Number 10-2005-0401 PROM revision A

PC/104p-IP
PC/104+ based IP Compatible
Carrier

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The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

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Connection of incompatible hardware is likely to cause serious damage.

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Product Description

PC104pIP is part of the Dynamic Engineering IP Compatible family of modular I/O components. The PC104pIP provides an IndustryPack® Compatible site in one PC/104+ slice. The slot is numbered "A" and the addresses updated to reduce the overall memory requirement of the card. The Dynamic Engineering Driver automatically compensates for the address changes.

ID, IO, INT, and MEM access types are supported for read and write cycles. The full 8 Mbytes of address space is allocated to the MEM space.

The PCI bus is 32 bits wide and most industry packs are 16 bit devices. Byte, word, and long word accesses are supported. Bytes can be to any address. Word accesses need to be word aligned. Long word accesses need to be long word aligned. Each of the access types has a one-to-one correspondence to the hardware. There are no "extra" accesses with the PC104pIP design.

A long word access to a 16 bit port will automatically be converted into two back-to-back IP accesses with the address incrementing between cycles unless the increment disable function is selected (see Slot control register description). In the increment disable case the hi or low address can be specified for the double access.

For a read, one 32 bit data word will be returned. For example a long word read to the ID space would yield $xx50xx49 for many boards as the "0" location has $49 and the next address has $50. The long word mode happens automatically when all 4 of the byte lane enables are detected asserted. The overall throughput is greatly enhanced with this mode of operation. Please note that the non-data bytes should be masked, as many IPs do not drive the "off byte".

The PCI bus is defined as little endian and many IPs have their register sets defined to operate efficiently with a little endian interface. The default settings on the PC104pIP are "straight through" byte for byte and D15-0 written to address 0x00 before D31-D16 written to address 0x02 when long words are written to 16 bit ports. Please note that any long word address can be used. The lower data is written to the lower address first, then the upper data to the upper address.   Each slot has a BS and WS control bit to allow Byte and Word Swapping to be performed to accommodate alternate IP and OS requirements.

Byte Swapping
16 bit ports
D15-8 ⇔ D7-0
D31-24 ⇔D23-16

Word Swapping will swap D31-16 with D15-0

If byte swapping is enabled and 0x1234 is written to an IP slot, then the IP will see 0x3412. If 0x12345678 is written to a 32-bit port then the IP will see 0x78563412. The "is written" is defined by the data on the PCI bus. Your software/OS may do its own conversion before the data gets to the PCI bus.

The byte and word swap controls are separated to allow the conversion to be used for big-little endian and for register mapping purposes. Each slot has separate controls for access to that slot.

The PC104pIP has a watch-dog timer function which completes the IP access if the IP does not respond within 7.6 uS. The watch-dog timer has a master status bit and an optional interrupt output. In addition to the master status each slot control register reports status for the bus error. Multi-threaded programs can tell if their hardware access caused the Bus Error even if other threads have accessed other hardware since the bus error was caused.

The slot is programmable for 8 or 32 MHz operation. The clocks are locked together and can be switched at any time. Hardware insures that the clocks switch basis on a clock period boundary to provide seamless operation.

The PC104pIP supports interrupts with separate mask bits. Two interrupts from the IP slot plus internal sources. An interrupt "force" bit is supplied to aid in software development. The bus error [watch dog timer] can also be an interrupt condition. The masked interrupts are tied together and connected to INTA on the PCI bus.

The PC104pIP has LEDs for power, access, and user functions. The three voltages from the IP slot are connected to three LED's. An additional 8 LED's are supplied which are controlled via the control register for user defined purposes. One LED is controlled by a timer circuit which is activated by acknowledge from the IP slot.

The power to the IP slot is individually filtered and fused for +5 and ±12. The fuses are rated at 2A on the 5V rail and 1.1A on the ±12V rails. The PC104pIP is designed to route maximum power. The power supply capabilities for your chassis may provide additional constraints. The slot filter has a separate RF filter, bulk capacitor, "self healing" fuse, and bipass capacitors. A bipass capacitor is located at each of the power pins on the PC104pIP with the bulk capacitor near the filter pin for optimum noise rejection, voltage hold-up and local filtering.
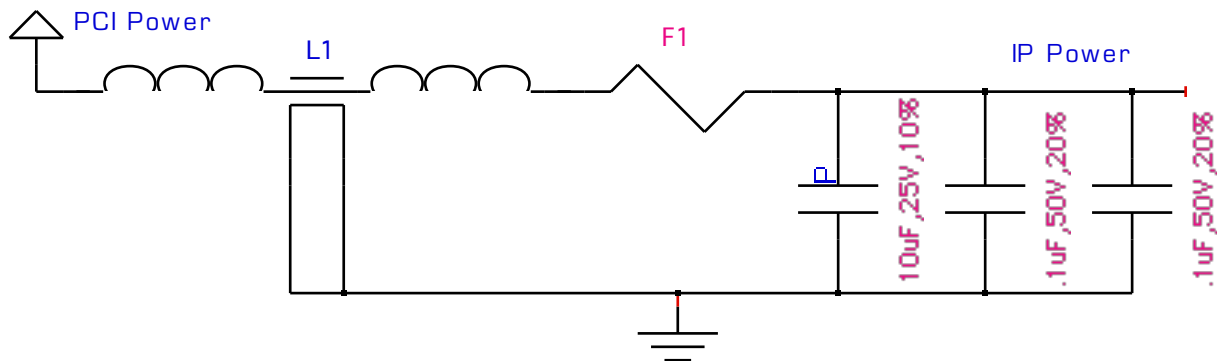
FIGURE 1   PC104PIP POWER FILTERING

 With the filter pin on each slot and bulk capacitor the IP is effectively isolated from the other hardware on the same supply rail. Additional work was done in layout to minimize the amount of cross-slot electronic noise. The FPGA uses 3.3 and 2.5V power which is derived from the 5V supply and bussed on mini-planes to the FPGA. The FPGA is effectively isolated from the IP slot by the regulators and additional filtering.

The PC104pIP is well behaved with low noise power provided to the slot. The PC104pIP is designed for analog and digital IP applications including data acquisition, instrumentation, measurement, command and control, telemetry and other industrial applications.

An 8 bit "dip switch" is provided on the PC104pIP. The switch configuration is readable via a register. The switch is for user defined purposes. We envision the switch being used for software configuration control, PCI board identification or test purposes. In addition the two bit positions [1,0] are used to select which of the 4 stack addresses to use – which PCI clock and which IDSEL to use plus the corresponding RQST and GNT. The upper 6 bits are available for user purposes.

Stack Address

XXXX XX00   INTA, CLK0, GNT0 , RQST0
XXXX XX01   INTB, CLK1, GNT1 , RQST1
XXXX XX10   INTC, CLK2, GNT2 , RQST2
XXXX XX11   INTD, CLK3, GNT3 , RQST3

The reset switch provided can be used to reset the IP devices without affecting the PCI bus. Power, PCI reset, and a control register bit also cause the IP Reset to be activated. The reset is controlled to be synchronous to the 8 MHz. clock. Alternatively, the IP-Debug-Bus card can be used for individual slot resets.

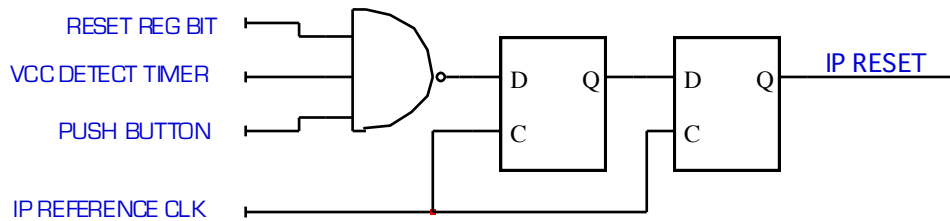
FIGURE 2   PC104PIP RESET CIRCUIT

The IO are brought to a 50 pin right angle header. The header is installed without ejectors to be PC/104p compliant max connector area. The ejectors can be installed by special request.

The PC104pIP conforms to the VITA standard for IndustryPack® Carriers. This guarantees compatibility with multiple IndustryPack® compatible modules.

The PC104pIP conforms to the PCI 2.2 specification and supports both 3.3V and 5V signaling levels. The PC104pIP is accessible in the memory space on the PCI bus. This guarantees compatibility with other PCI compliant hardware – most PC's.

The PC104pIP is not PC/104+ mechanically compliant. The IP Module is longer than the PC/104p. The connector area is utilized to expand the size of the PC/104p to accommodate the larger IP Module. The PC104pIP does stay within the PC/104p definition with the connector area added. With a chassis that allows for the full connector area, the PC104pIP will fit. The PC104pIP will install into a standard PC/104+ stack as long as the "overhang" is taken into account.

The thickness of the IP is also an issue to be examined. The allowable height in the component area is .345" on the top and .190" on the rear. A type I IP module is .534 thick when mounted. If the stack member above the PC104pIP is clear on the bottom then the stack will "just fit" with 1 mil clearance. PC104pIP has no components on the "bottom" to interfere with other PC104pIP cards making them stackable together. If the other system cards use the bottom area above the IP then the PC104pIP will need to be the "top" of the stack or connector extenders used to expand the gap.

The J1/J2 connectors are provided to pass through the ISA signals if they are present in the stack. The PC104pIP does not utilize any if the J1/J2 pins. The ISA connectors can be left off it that is preferred. Please call our sales department with any special build requests.

The PCI interface is integrated with the IP interface providing superior performance over designs relying on a separate PCI interface device. In addition to access speed, the higher level of integration results in fewer initialization steps and requirements, more flexibility in operation, a higher MTBF, and less complex software with only one Base Address [BAR] to deal with.

If your project can benefit from a "non-standard" implementation, or features that we have not thought of, or implemented yet please let us know. The Xilinx has room. For example; if your project will use IP's that can operate at 33 MHz instead of 32, then we could synchronize the IP and PCI clocks and save several synchronization steps.

Wired but not yet implemented. (1) All of the DMA control signals are available for a future revision to implement.

Wired and User implemented. The IP Strobe signal is connected from the IP slot to a pin header to allow for inter-slot user defined communications. The IP specification does not define what the strobe can be used for. The header is rarely used. If you need it please add –stb to your order number and we will install the header for you. Standard .025" sq. posts suitable for wire-wrap inter-connection.

On the IP Slot the Strobe signal is connected to pin 46.

Strobe Pinout on Header

TP1
1   STB B
Figure 3   PC104pIP Strobe connection table

Theory of Operation

The PC104pIP is used to bridge from PCI to IP bus specifications. The PCI bus will be the master in most cases with the IP being accessed for read or write cycles. The PCI accesses are handled at the lowest level by the PCI core.

The PCI bus provides multiplexed address and data plus control lines. The data is separated from the address, and the control lines are decoded to provide the inputs to the IP Interface state machines. The address is tested to determine which type of access to implement. The IP control strobes are generated. When acknowledge is received the cycle is terminated back to the host. The PCI bus will see a retry mode while the access is taking place and "disconnect with data" when the cycle is completed.

Feature List
• PCI Universal Voltage [3.3 or 5V signaling]
• Integrated PCI ⇔ IP conversion for faster access
• IP compatible slot
• Full ID, IO, INT, and Memory space allocated
• 8 or 32 MHz operation
• byte, word, long word access. 32 bit access to 16 bit slots with static or incrementing address.
• byte and word swapping for little endian – big endian conversion
• Bus error abort response with slot status
• 1:1 50 pin header
• IP Reset Switch
• 8 position "DIP Switch" – slot identification when multiple PC104pIPs are in your system or for user defined purpose(s)
• 8 User LEDs, 3 Power LEDs, Access LED
• Fused Filtered Power with resetable "self healing" fuses.
• Windows®10 Driver available. Generic IP interface included with driver to support your IP. Dynamic Engineering driver development available for customized IP support. [please download the separate Driver manual]
• Linux Driver available.

If you develop a driver for one of our products or a third party IP child driver and are willing to allow others to use it; we will add it to the web site as a free of charge download and, if desired, give credit to the author.

As Dynamic Engineering adds features to the hardware we will update the PC104pIP page on the Dynamic Engineering website.

Installation

***PC104pIP and the IP to be mounted should be treated as static sensitive
hardware***. The technician should be properly grounded; the mounting and installation
process performed at a static free workstation.

The PC104pIP can be installed into any PC/104+ "slot" with connector capability. The
mounting hardware will securely retain the PC104pIP within the chassis. The
PC104pIP with type1 IP Modules installed is PC/104+ compliant[1] for height, length and
width. Adjacent slots can be filled with multiple PC104pIP cards.

IndustryPack®s are installed by pushing the mezzanine card onto the connector pair on
the PC104pIP. The slot is clearly marked. The IO connector is located near the top of
the PC104pIP and the IP Bus connector at the opposite edge. The IP connectors are
keyed making orientation error proof.

The IP mounting kit can be utilized to secure the IP to the PC104pIP. Each Dynamic
Engineering IP sold comes with a mounting kit. If you need a replacement or your IP
comes from another manufacturer please order IP-MTG-HW. 1 kit per IP. The kit
includes stainless steel hardware – screws and standoffs.
http://www.dyneng.com/IPHardware.html

If more than one PC104pIP is to be installed into the same system – visible on the PCI
bus then the dipswitch can be set to different positions on each card. The software can
use the dipswitch setting to identify which PC104pIP is allocated which address space
and associate specific IP/cables with that PC104pIP so there is positive automatic
control of your system configuration. The Dynamic Engineering Driver makes use of
this feature to allow multiple PC104pIPs to be used in the same system without
identification challenges. The switch also changes the IDSEL and clock used within the
stack to prevent hardware level conflicts.

---

[1] Please refer to mechanical discussion for more details. The IP Module will use the rear component
space of the slice mounted above.

Address Map

```
PC104pIP_intreg_base      0x00000000 // base control register
PC104pIP_intreg_ip        0x00002000 // slot  specific clock and interrupt
PC104pIP_intreg_dswitch   0x00006000 // User Switch read back port
PC104pIP_intreg_int       0x00007000 // Interrupt status read-back

PC104pIP_id_st            0x00140000  // starting address of slot ID space

PC104pIP_io_st            0x00240000  // starting address of slot IO space

PC104pIP_int_st           0x00340000  // starting addr of slot INT space

PC104pIP_mem_st           0x00800000 // starting addr of slot  MEM space
PC104pIP_mem_en           0x00FFFFFF  // end address of slot  MEM space
```

FIGURE 4   PC104PIP ADDRESS MAP

The address map is for the local decoding performed within PC104pIP. The addresses are offsets from a base address. The host provides the base address and interrupt level. Your software will need to concatenate the base address + PC104pIP address + IP Local address to create a pointer to each programmable feature on your IP.

Programming

The address map will get you to the IP. The IP board description will provide the local addresses. If you are in a Windows or Linux environment we recommend using a Dynamic Engineering Driver for the carrier and IP. Complete information is provided within this manual to allow customers who use another OS or want to write their own interface to do so.

Dynamic Engineering can write a driver for your IP to interface with our carrier(s) even if it is not "one of ours". Please contact engineering@dyneng.com with your requirements if you are interested in this service.

The host system will search the PCI bus to find the assets installed during power-on initialization. The VendorId = 0x10EE and the CardId = 0x0019 for the PC104pIP. Interrupts are requested by the configuration space. PCIView and other third party utilities can be useful to see how your system is configured. The VendorId and CardId parameters are used by the OS to identify the card, and in some cases launch the plug and play installation process. The interrupt level expected and style is also set in the registry.

Once the initialization process has occurred and the system has assigned an address range to the PC104pIP card, the software will need to determine what the address space is. We refer to this address as base0 in our software.

The next step is to initialize the PC104pIP. The default of no interrupts enabled and 8 MHz operation will be valid in many cases. The base register for the PC104pIP and specific slot register can be initialized to change the default parameters to suite your requirements. Please refer to the register map definitions for more information.

Access to your installed IP is done by accessing base0 + slot address + IP offset. The slot address is defined in the memory map. For example to read your IP in slot B IO space: *(base0 + PC104pIP_iob + ip offset) = data. Each slot and memory type [IO, ID, INT, Mem] has a unique address space for 4 defined address spaces plus the PC104pIP internal address space. The internal registers are defined in the following pages.

The PC104pIP has an integrated PCI interface with IP bridge. The integrated approach simplifies programming with only one base address and fewer parameters to have to initialize. The integrated approach is also a faster access approach leading to higher performance in your system.

Higher performance for your system can be achieved by matching the IP register model to the OS and user software model that you are using, selecting the optimal IP reference clock rate and access types.

The PC104pIP has clock selection for the IP Slot. The access time is reduced when the IP clock rate is set to 32 MHz. The PC104pIP can handle any mixture of clock requirements. Make sure that the IP in the slot can handle the higher rate.

The PC104pIP can handle byte, word and long word accesses from the PCI bus. 32 bit accesses to 16 bit ports will be converted to double accesses. The Byte Swap [BS], Word Swap [WS], Address Increment, and Word High allow the accesses to be customized for the IP installed for optimum performance. 32 bit accesses to 16 bit ports are faster than individual 16 bit accesses and frequently easier to write software for. For example if your IP has a 24 bit port with 16 bits in one register and 8 in the next you can write all 24 with one 32 bit access. With word and byte swapping you can account for the organization of the registers on the IP.

Some IPs convert 16 bit accesses to double 8 bit accesses – IP-QuadUART for example. If your IP has 16:8 conversion then you can write 32 bits and get 4 – 8 bit writes to your IP in one access.

Read the IP manual and see what strategy is best to communicate with that card then adapt the settings on the PC104pIP to optimize your accesses to that IP.

Register Definitions

PC104pIP_intreg_base

[$00 Main Control Register Port read/write]

```
                         CONTROL  REGISTER 0

            DATA BIT                DESCRIPTION

              31                    Reset 1 = reset IPs 0 = normal
            30-14                    spare
              13                    INT FORCE 1 = FORCE 0 = NORMAL
              12                    Master INT EN 1 = ENABLED 0 = DISABLED
              11                    spare
              10                    spare
               9                    Bus Error Int/Status Clear
               8                    Bus Error Int En
               7                    LED7 1 = ON 0 = OFF
               6                    LED6
               5                    LED5
               4                    LED4
               3                    LED3
               2                    LED2
               1                    LED1
               0                    LED0
```

FIGURE 5   PC104PIP CONTROL PORT

Reset when set causes a reset to the IP slot. Reset is active as long as the Reset signal is asserted. Reset is synchronized to the IP clock per the IP interface specification. The duration is controlled by the user software. 200 mS is a suggested minimum time to enable for resetting purposes. In addition there is a device on board which causes an IP reset of 200+ mS when a power transition to the powered on state is detected.

LED7-0 are the user LED's situated at the right side of the card near the IP Slot. Each LED can be activated by setting the corresponding data bit and deactivated by clearing the same bit. The LEDs are aligned on a nibble basis: 0x12 would be   off off off on   off off on off

Spare means undefined, and is suggested to be written as '0' to allow for commonality with future enhancements.

INT FORCE will, when set, cause INTA [selected to INTA, INTB, INTC or INTD with the selector switch] on the PCI bus to be asserted. This bit can be useful for software debugging. Set this to simulate an IP interrupt when the hardware is not available. The master interrupt must be enabled to have an effect.

Master Interrupt Enable must be set to allow the IP or other interrupt conditions to become an interrupt on the PCI bus. 1 = enabled. 0 = disabled or masked.

Bus Error Int En when '1' allows the bus error detection circuit to cause an interrupt to the host when a Bus Error is detected. The status is available on the Interrupt status register. When '0' the status is still valid but no interrupt is generated when a bus error is detected. The bus error is detected when an access to one of the IP slots is not responded to by IP hardware within the time-out period of approximately 7.3 uS. The bus error circuit is always enabled and automatically responds as if the IP had responded. The data read will typically be $FF if the IP is not driving the bus for a bus error read. For a bus error during a write, the write should be assumed to not have taken place. The host will not know that the bus error has taken place unless the host checks the status. The interrupt can provide a prompt to check the status during operation. During initialization if the software is checking to "see" what is installed or what address range is valid on an IP then the status can be polled to see if the IP responded.

Bus Error Status / INT Clear when '1' will clear the status bit and interrupt request [if enabled]. The Clear bit needs to be reset to '0' to be able to capture the next Bus Error. The bus error timer hardware operates independent of clearing the status and will continue to monitor and intercede whether the status is read or cleared. Each of the slot registers has an additional status bit to identify which slot caused the bus error. The master status can be used to identify the interrupt type and the local registers to identify the source.

PC104pIP_intreg_ip

[$2000 Slot Control Register Port read/write]

Slot CONTROL   REGISTER

DATA BIT	DESCRIPTION
17	IRQ1 (read only)
16	IRQ0 (read only)
15-9	Undefined
8	bus error status/clear
7	word swap control
6	byte swap control
5	Interrupt Enable 1
4	Interrupt Enable 0
3	High Word Access
2	Increment Disable
1	spare
0	Speed Control 1 = 32 MHz, 0 = 8 Mhz

FIGURE 6   PC104PIP SLOT CONTROL PORT

Speed Control selects the slot clock speed. 1 = 32 MHz. 0 = 8 MHz. Clock selection change can be made at any time. Each slot has a separate speed control bit. Default is 8 MHz.

Increment Disable, when '1', turns off the address increment that normally occurs between 16-bit IP cycles when a 32-bit PCI access is performed. This is useful if, for instance, a FIFO is mapped to a single IP address since it allows double IP accesses to the same address with a single PCI transfer. All types of access are affected (i.e. MEM, IO, INT, and ID). Only 32 bit accesses are affected.

High Word Access controls which 16-bit word is accessed when the Increment Disable is asserted. When '0' the lower word is accessed twice, when '1' the upper word is accessed twice. This bit only has an effect when the Increment Disable bit is '1'. For correct functioning, please make sure the PCI access is on a long-word boundary.

Interrupt Enable 0,1 individual masks for the 2 interrupts from the IP slot. 0 corresponds to INT0 and 1 corresponds to INT1.

Byte Swap when '1' causes the byte lanes to be swapped. For a 16-bit access the upper byte is swapped with the lower byte. For a 32-bit access to a 16-bit

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port the upper and lower of each word are swapped. Byte Swap when '0' provides the data on the same byte lanes that the PCI bus provides them on. Byte Swapping can be used in conjunction with the Word Swap feature for big endian ⇔ little endian conversion.

16 bit ports
D15-8 ⇔ D7-0
D31-24 ⇔D23-16
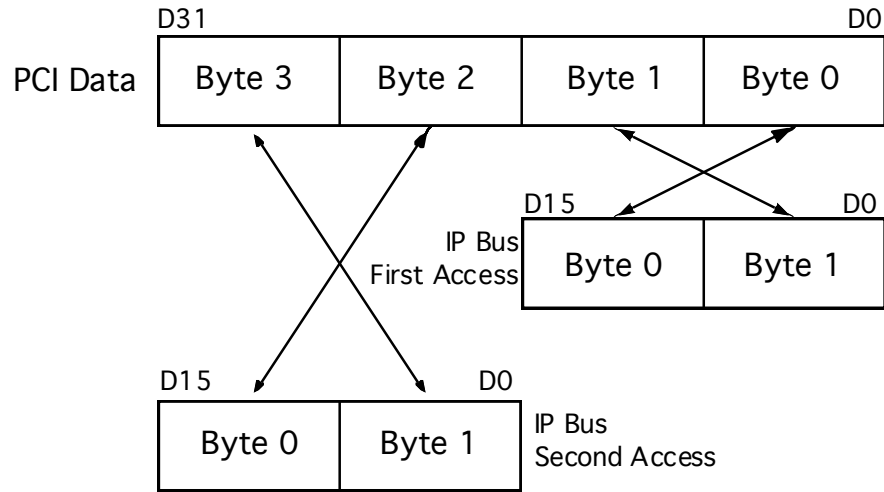
FIGURE 7   PC104PIP 16 BIT BYTE SWAPPING

Word Swap when '1' will cause the upper and lower words to be swapped. Data written to PCI D15-0 will be driven onto the IP bus as if it originated on D31-16. Word Swap when '0' leaves the data on the PCI word definitions.

The IP bus interface state-machine will move data from D15-0 to the "0" address and from PCI D31-16 to the IP "2" address. IP addresses are word based for non-32 bit capable accesses [even with 32 bit transfers]. The PCI bus will write data to either the upper or lower words and apply the corresponding CBE byte lane strobes. The PC104pIP hardware will translate the data to D15-0 on the IP.

Word swapping can be used effectively for big endian ⇔ little endian translation and to accommodate IPs with registers that can be more effectively accessed in reverse order. For example: if the IP registers are organized with the MS data at address 0x00 and the LS data at 0x02 then a single 32 bit write can be made to 0x00 with address incrementing enabled and word swapping enabled so that the PCI D31-16 data is written to IP 0x00 and the PCI D15-0 data is written to IP 0x02. If the IP registers have data 16 bits or less then word swapping will not be

needed.

With the combination of Byte and Word Swapping plus address definition any byte/word can be direct to/from any destination. Big ⇔ little endian issues can be resolved and IP architecture optimized for software access.

The **bus erro**r bit is a status bit with a write clear. The clear is active at the time of the write only and does not need to be reset. If the bus error bit is set when the register is read then a bus error has occurred on this slot. Once set the bit will remain set until explicitly cleared by writing a '1' to this bit position.

IRQ0,1 are status bits showing the state of the interrupt request line from the IP. The state of the interrupt request is inverted. '1' = interrupt active, '0' = no interrupt.

PC104pIP_intreg_int

[$7000 PC104pIP interrupt register read only]

```
                    CONTROL  REGISTER 0

            DATA BIT                DESCRIPTION


            31-23                   undefined
              22                    Bus Error 1= occurred 0 = none
              21
              20
              19
              18
              17
              16
              15                    UNMASKED B1 1 = SET 0 = NOT SET
              14                    UNMASKED B0
              13
              12
              11
              10                    INTRN 1 = SET, 0 = NOT SET
               9
               8
               7
               6
               5
               4
               3                    MASKED B1
               2                    MASKED B0
               1
               0
```

FIGURE 9   PC104PIP INTERRUPT STATUS PORT

The interrupt requests from each of the IP slots are available as status from this port. The interrupt requests are inverted to make them active high for software usability. The requests are available in a masked and unmasked form to allow polling with the PCI interrupt masked off. When an interrupt is detected this register should be accessed to determine the source or sources and then appropriate action taken to clear the interrupt at the IP or clear the mask on PC104pIP.

The PC104pIP provides direct access to the interrupt space. If the IP causing the interrupt requires an interrupt vector fetch to clear the interrupt then the appropriate INT space should be accessed. Address bit A1 selects between Int0 and Int1. A1 follows the word address to allow access to both INT0 and INT1 clearing addresses within the INT space.

Most IPs support having an interrupt vector. The vector associated with INT0

can be accessed from base0 + PC104pIP_int[slot]_st + 0x00. The vector associated with INT1 can be accessed from base0 + PC104pIP_int[slot]_st + 0x02. If the IP does not require a Vector fetch to clear the interrupt then proceed with IO or other accesses as necessary.

The Bus Error status bit is set high when a Bus Error is handled by the internal watch dog timer circuit. The status will stay high until cleared with the Bus Error Int / Status Clear bit in the base control register. The Bus Error status bit is or'd into the interrupt request logic and if enabled will cause a level sensitive interrupt to the host. The interrupt will remain asserted until the status is cleared. The PC104pIP Base register contains the enable and clear for the bus error logic.

PC104pIP_intreg_dswitch

[$6000 User Switch Port read only]

DipSwitch Port	
DATA BIT	**DESCRIPTION**
7..0	Sw7..0

FIGURE 10   PC104PIP USER SWITCH PORT

The user switch is read through this port. The bits are read as the lowest byte. Access the port as a long word and mask off the undefined bits. Read only. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.
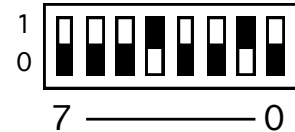
Stack Address

XXXX XX00   INTA, CLK0, GNT0 , RQST0
XXXX XX01   INTB, CLK1, GNT1 , RQST1
XXXX XX10   INTC, CLK2, GNT2 , RQST2
XXXX XX11   INTD, CLK3, GNT3 , RQST3

The switch can be used for any user purpose or to identify a particular PC104pIP in a system with more than one card installed. Dynamic Engineering Driver software uses the switch for slot identification. The lowest two bits determine the INT(A,B,C,D), CLK(0,1,2,3), REQ(0,1,2,3) and GNT(0,1,2,3) to use within the PC/104+ stack.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID 0x10EE and CardId 0x0019 and an interrupt level. If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltages to the PC104pIP when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the IP's installed onto the PC104pIP than the PC104pIP itself, and it is smart system design when it can be achieved.

Connector definition. The "IO" connector on the IP is tied 1:1 to the IO connector on the PC104pIP. The IO connector is a standard 50 pin header; ribbon and discrete wire compatible. Please refer to the diagram near the end of the manual.

IP Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the IP Module Logic Interface on the PC104pIP slot. Also see the User Manual for your IP board(s) for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSEL*	4	29
D1	DMA-reserved	5	30
D2	MEMSEL*	6	31
D3	DMA-reserved	7	32
D4	INTSEL*	8	33
D5	DMA-reserved	9	34
D6	IOSEL*	10	35
D7	reserved	11	36
D8	A1	12	37
D9	DMA-reserved	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	INTREG0*	17	42
D14	A4	18	43
D15	INTREQ1*	19	44
BS0*	A5	20	45
BS1*	Strobe	21	46
–12V	A6	22	47
+12V	Ack*	23	48
+5V	reserved	24	49
GND	GND	25	50

NOTE 1: The error signals is defined by the IP Module Logic Interface Specification, but not used by this Carrier. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked on the carrier.

FIGURE 11   PC104PIP LOGIC INTERFACE

Construction and Reliability

IP Modules were conceived and engineered for rugged industrial environments. The PC104pIP is constructed out of 0.062 inch thick high temp ROHS compliant FR4 material.

Through hole and surface mounting of components are used. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IP Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amps per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP Module can be secured against the carrier with the connectors. If more security against vibration is required then IP mounting kit can be used to attach the IP to the carrier. Dynamic Engineering has mounting kits available if your IP did not come with one.

The IP connectors are secured to the carrier with the mounting standoff and screw.   Using the standoffs to secure the carrier side IP connectors to the carrier helps to reduce the strain on the soldered joints on the SMT carrier connectors. Using a side-to-side rocking motion to remove IP's is also preferred over rotating in the long direction.

http://www.dyneng.com/IPHardware.html

MTBF

The PC104pIP has been modeled with Belcore reliability prediction software. The MTBF is reported as 1.37 M Hours. GB 25C.

Thermal Considerations

The PC104pIP design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. The installed IP Modules may require forced air cooling. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-3840 fax
support@dyneng.com

Specifications

Logic Interfaces: IP Logic Interface, PCI Interface -33 MHz. 32 bit, universal signaling

Access types: IO, ID, MEM, INT IP Spaces supported via PCI bus accesses

CLK rates supported: 8 MHz or 32 MHz IP reference clock selectable
                               33 MHz. PCI

Software Interface: Control Registers, and Installed IP. Programming procedure
                               documented in this manual

Access Modes: LW, Word or Byte to IP registers. LW can be converted to two word
                               accesses. LW to Internal PCI Interface Control registers. Bus error
                               detection and handling.

Access Time: Typical access time with 32 MHz. IP and double access mode is 500 nS.

Interrupt: 2 Interrupts per IP slot with separate enables. Programmable Bus error
                               interrupt.

DMA: No DMA Support implemented at this time

Onboard Options: All Options are Software Programmable

Interface: Right angle 50 pin Header Connector

Dimensions: Modified PC/104+ board [Connector area utilized]

Construction: FR4 Hi Temp Multi-Layer Printed Circuit, Through Hole and Surface
                               Mount Components. Programmable parts are socketed.

Power: RF filtered and fused to IP slot. Resettable "self healing" fuses.

User   8 position software readable switch
                               8 software controllable LEDs

Other LED   LEDs (3) on slot power (±12,5) LED used to show IP
                               acknowledge to access – 1 per slot.

Slots   Single wide IP slot

Temperature Range   --40 +85 C

Temperature Coefficient: 2.17 W/^{o}C for uniform heat across Carrier

MTBF   1.37 M Hrs. GB 25C

Order Information

PC104pIP   http://www.dyneng.com/pc104p_ip.html
                            PC104p adapter for IndustryPack Modules. PCI bus
                            used. ISA connector is stack through

PCI-104IP   PCI-104 adapter for IndustryPack Modules.

-CC   Add conformal coating

-ROHS   Add ROHS processing.

IP-DEBUG-BUS   http://www.dyneng.com/ipdbgbus.html
                            IP test points, reset switch, fused power, quick switch
                            isolated interface lines to allow hot swapping of IP cards.

IP-DEBUG-IO   http://www.dyneng.com/ipdbgio.html
                            Isolate the IO connector to help with debugging. 50-pin
                            header for system cable connection. 50 test points
                            suitable for wire-wrap to allow loop-back connections.
                            Locations for power and user circuits.

HDRterm50   http://www.dyneng.com/HDRterm50.html
                            50-pin header to 50 screw terminal converter with DIN
                            rail mounting.

PC104p-Chassis   http://www.dyneng.com/pc104p_chassis.html
                            extruded chassis for PC104p, PCI-104, PC104, PCIe104
                            applications. Rugged with mounting flange, front and
                            rear panel gaskets.
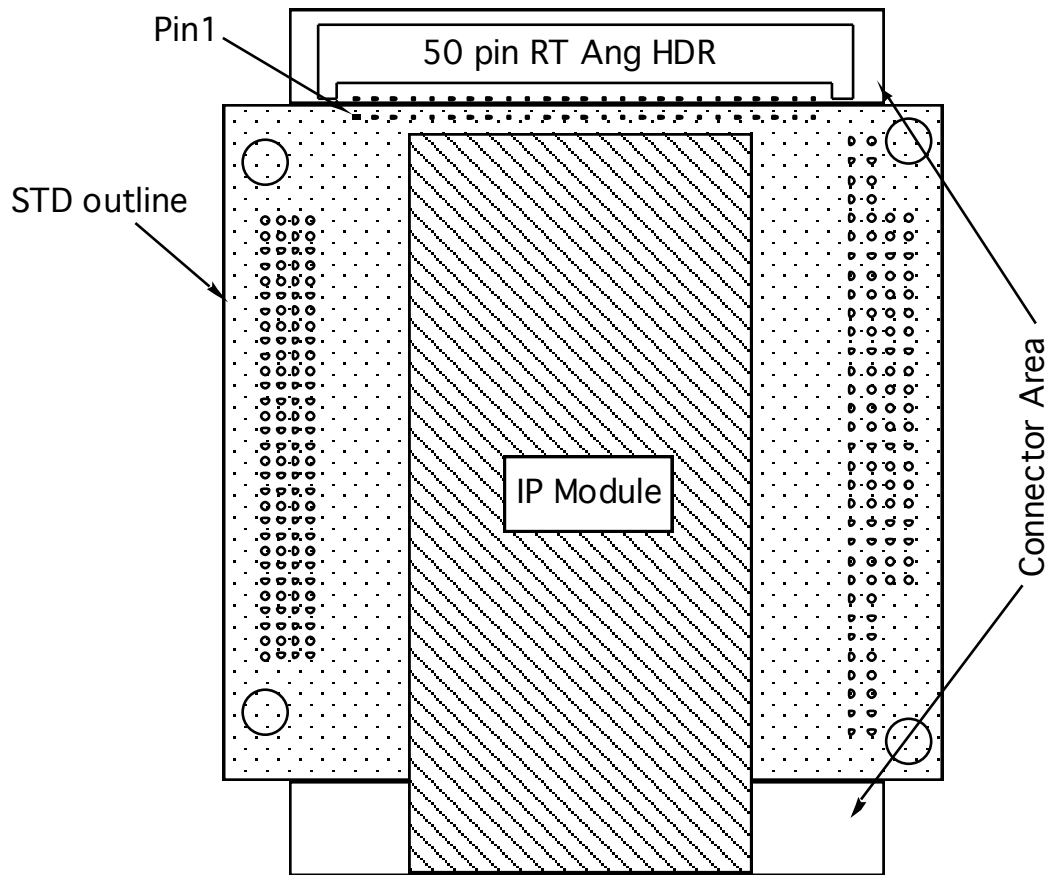
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Pin1

STD outline

50 pin RT Ang HDR

IP Module

Connector Area

FIGURE 12

PC104PIP LOCATION REFERENCE

PC104PIP CONNECTOR REFERENCE

The PC104p4IP has 1 IP slot and 1 header connector.

The wiring is 1:1 from the IP IO connector to the PC104pIP header connector. The connectors are numbered to match standard ribbon cable as shown in the figure to the right.

Pin 2
Pin 1
50 Pin Header

Pin 50
Pin 49

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