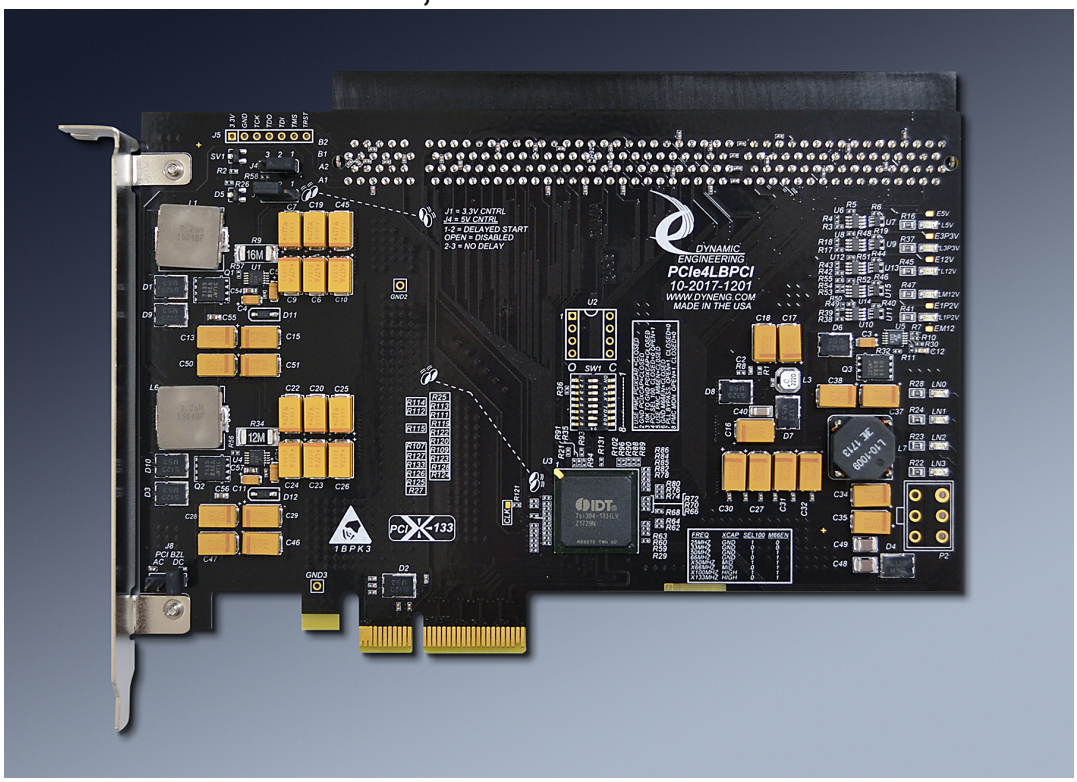
DYNAMIC ENGINEERING

150 DuBois St. Suite C
831-457-8891 **Fax** 831-457-4793
http://www.dyneng.com
sales@dyneng.com
Est. 1988

User Manual

PCIe4LBPCI- 4 PCIe Lane

PCIe ⇔ PCI, PCI-X 1 Position Riser



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PCIe4LBPCI
PCIe to PCI Riser

Dynamic Engineering
150 DuBois St Suite C
Santa Cruz, Ca. 95060
831-457-8891
831-457-4793 FAX

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none at this time

Product Description

PCIeB4LPCI is part of the Dynamic Engineering PCI Express and PCI Compatible family of modular I/O components. PCIe4LBPCI adapts a PCI device to PCIe. **[PCIe 4 L**ane **B**ridged adapter to **PCI**]

The main purpose is to allow testing or use of a PCI card in a chassis without PCI slots. PCI and PCI-X compatible on the PCI socket mounted to the top of the card. The bezel of the installed PCI card will snug in behind the bezel of the PCIe4LBPCI to provide a friction hold on the installed device.

Any IO from the installed PCI device will be fully accessible with the PCI device almost completely out of the chassis.

PCIe4LBPCI uses up to 4 PCIe lanes to operate with PCI-25, 33, 50, 66,100 or 133 speeds.

PCIe4LBPCI 4 lane min. backplane connector size up to 4 lanes used With PCIeB4LPCI => 4, 8, 16 or 32 lane connectors can be used.

Unlike PCI, the PCIe specification provides for 12V power [only] to be used by the Express module. A minimal amount of 3.3V is available from the Express connector but not enough to power typical PMC devices. Local power supplies operate from the +12V to create the rest of the PCI voltages [-12, 5V, 3.3V]. The 5V and 3.3V power supplies can source 9.5A each and the –12V is designed for 4A, but effectively limited by the single pin assigned by the PCI specification.

Voltage monitors check the power supplies are operating correctly and illuminate LED's when in regulation [under and over voltage checked].

The transparent bridge does not require any software interaction. Your PCI drivers will work without modification when hosted by the PCIeB4LPCI. The bridge can provide higher bandwidth for DMA transfers if some settings are adjusted.

Special features:

- PCIe Compliant 1-4 lane design based on highest performance bridge TSI384.
- PCI, PCI-X compliant on secondary [PCI] bus
- LED's on plus 12V, minus 12V, plus 5V, plus 3.3V plus bridge power. Each is controlled by a voltage monitoring circuit. If illuminated the voltages are within tolerance.
- LED's on PCIe Lane Status (LN0-3)
- Local power supplies for +5, 3.3 and M12
  The 5V and 3.3V supplies can be disabled, delayed, or instant on.
- VIO set to 3.3V.
- 32 or 64 bit operation
- 133, 100, 66, 50, 33 or 25 MHz operation.
- Front panel connector access through PCI bracket
- Optional JTAG programming support
- User Selection for AC, DC and open for PCIe Bezel.

The PCIe4LBPCI is ready to use with the default settings. Just install the PCI device onto PCIe4LBPCI. There are a few settings to optimize performance.

DipSwitch Settings

Please note that the switch numbering and 'C' and 'O' definitions are per the silk screen.

The dipswitch is numbered SW1 and is located near the center of the board. SW1 controls the Bridge operation. UP = Closed and DOWN = Open.

For forced operation use the following settings: Note that the PCI must be capable of operating at the selected frequency. To truly force independent of the PCI open switch 1,5

Mode and Bus Rate	PCI_PCIXCAP	PCI_SEL100	PCI_M66EN
switches	**1,2,3**	**4**	**5,6**
PCI 25 MHz	C,C,C	O	C,C
PCI 33 MHz	C,C,C	C	C,C
PCI 50 MHz	C,C,C	O	C,O
PCI 66 MHz	C,C,C	C	C,O
PCI-X 50 MHz	C,O,C	O	C,O
PCI-X 66 MHz	C,O,C	C	C,O
PCI-X 100 MHz	C,O,O	O	C,O
PCI-X 133 MHz	C,O,O	C	C,O

For automatic operation use the following settings

Mode and Bus Rate	PCI_PCIXCAP	PCI_SEL100	PCI_M66EN
switches	**1,2,3**	**4**	**5,6**
Automatic selection	C,O,O	C/O	C,O

Please note that switch 4 is used to select between the upper and lower frequency at each frequency level (25/33, 50/66, 100/133)

Special selections for the Tsi Bridge
For more information please refer to the IDT[Tundra]® documentation

The DIPSWITCH has 8 switches. Normal IC pin numbering is used; 1-16 comprise switch 1, 2-15 => switch 2 and so forth.

Factory default is “C O O C C O O O” C= closed [up], O = Open [down].

Position 1 corresponds to S_PCIXCAP and P_PCIXCAP. When closed the signals are tied together. When open the signals are isolated. The S_PCIXCAP is tied to the PCI position PCIXCAP signal. P_PCIXCAP is tied to the Bridge. When connected together automatic operation is enabled; the PCI and Bridge negotiate for the frequency automatically. Setting to open isolates the two devices, and allows the user to override the PCI set-up.

DIPSWITCH pins 16, 15, and 14 are tied together to allow the user to control the bridge side of PCIXCAP with options on switches 1, 2, 3. Connecting the signals through on **switch 1** and leaving switches 2, 3 open is the default setting for standard operation.

Closing **switch 2** can be used to ground the Bridge side PCIXCAP signal and selectively ground the PMC version of the signal if position 1 is also closed. This has the effect of forcing the speed range to be 25-66 MHz.

Closing **switch 3** can be used to create an intermediate voltage on the PCIXCAP signal on the Bridge and optionally on the PCI side. There is a 56KΩ pull-up to 3.3 on the secondary side of the switch. Closing switch 3 adds the pull-down resistor – 10KΩ to ground. PCI's with PCI-X 66 capability should have the 10 KΩ pull-down on the PCI making the intermediate voltage selection automatic.

PCI cards operating at PCI 66 MHz [not PCI-X] will ground the PCIXCAP signal and leave M66EN high. The ground from the PMC will override the switch 3 setting unless switch 1 is open.

Switch 4 when open leaves PCI Select 100 pulled up to 3.3 though an 8.2KΩ resistor. If the switch is closed the signal is tied to ground. PCI Select 100 is used to toggle between 100 and 133 or 50 and 66 or 25 and 33. The default selection is closed to allow the PCI to select 33, 66, or 133 MHz.

Switch 5 and **Switch 6** correspond to S_M66EN and P_M66EN respectively. When Switch 5 is closed and Switch 6 is open the signals are connected together with a light pull-up on each side. This is the default setting. When Switch 6 is closed the Bridge side is forced to ground – low speed operation.

When open the signal is '1' assuming that the PMC does not pull the signal down. S_M66EN/P_M66EN acts as an open drain signal with any of the nodes capable of reducing the clock rate and all nodes required to operate at the higher rate. Select the secondary side [PMC] PCI bus frequency. With the PCIe to PCI bridge the PCI clock is not related to the PCIe rate. The switches and card pin

strapping control the frequency. Tying the M66EN between the bridge and PMC plus doing the same for the PCIXCAP signal will allow for automatic clock selection based on the PCI/PCI-X specifications.

Position 7 corresponds to PLL_BiPass. When closed the signal the PLL is bipassed. When open the PLL is engaged. Default is open for PLL operation.

Position 8 is spare for this design

Interrupts

Interrupts from the PCI are routed from the PCI to the primary PCIe bus. INTA through INTD are mapped indirectly to the bridge where the interrupt requests are converted into PCIe control words and sent to the host computer. The host will respond over PCIe as programmed by the user software to deal with the interrupt. The operation is transparent to software as if the transaction happened over a PCI bus.

IDSEL

The IDSEL is set to AD20 for the PCI slot [secondary PCI].

Power supplies

PCIe has one glaring weakness… not enough power to the main PCIe connector for the smaller lane count boards. 12V, 3.3V, and 3.3V AUX are available on the backplane connector. PCIe4LBPCI uses the 12V and 3.3V AUX. The 3.3V rail is used for the bridge and not connected to the PMC. The PCIe 12V is also used to generate the 1.2V for the Bridge.

12V is Diode coupled to an optional second power connector [P2] located at the rear of the card. For applications requiring more than ~60W total power consumption the rear connector should be added [option –AP].

The 12V rail is tied to PCI 12V input and to the power supplies that generate the M12, 5V, 3.3V.

The 12V input rail at the gold finger connector is limited to about 5.5A max. 66W is the maximum input power. The power supplies have been measured to be about 90% efficient leaving 59.4W for internal use. The Tsi384 can use up to 2W leaving a minimum of 57.4W for the PCI.

The 5V and 3.3V supplies can generate 9.5A each – exceeding the capacity of the 12V input rail. Minus 12 has excess capacity and should be limited to 1A due to pin limitations on the PCI connector. +12V also shares this limitation.

For designs using less than 5A on the 5V and 3.3V rails and operating in a “lab” environment no additional cooling is required. With loads approaching 5A and or operating at higher temperatures forced air cooling is required. The full 9.5A may require additional airflow to the rear of the card depending on the operational temperature etc.

The FET’s use the PowerPAK package with the Drain tied to a pad on the bottom of the part allowing direct thermal contact. The improved package reduces the thermal resistance sufficiently to move the max no air flow current rating. In addition the inductor and FET have improved characteristics allowing for a max

of 9.5A.

3.3 AUX is directly routed to the PMC on the 3.3V AUX pin.

Many implementations will stay within the 57.4W limitation. For those designs needing the **extra** power; add the –AP option to your order to have the 6 position Alternate Power connector installed. The connector is compatible with standard PC power supplies. 2x3 array with locking mechanism.

J1 controls the 3.3V supply and **J4** controls the 5V supply. With no shunt installed the power supplies are disabled. If your PCI does not use the 3.3V or 5V power it is recommended to remove the corresponding shunt. Please note: the corresponding LED will go dark since the power is out of tolerance in this configuration. When 1-2 are connected the power supply is enabled with a delayed start-up. When 2-3 are connected the power supply is enabled without a delay.

The headers are labeled in the silk-screen. The pins are also labeled in the silk to support the on-off and delay type selection.

The delay waits for the +12 to reach approximately 5V before starting a supervisor circuit timer. The circuit adds an additional delay before enabling the power supply. The delay can reduce the system in-rush requirement. Please note: in some systems the enumeration happens early and the installed PCI device may need the instant on setting to be configured in time to be enumerated correctly.

You can see the effect by delaying one supply and not the other, powering on and looking at the monitor LED's.

P2 Pinout

NAME	P2
GND	4,5,6
+12	1,2,3

P2 = -AP option PCIe power cable connector

J8 Pinout

J8 is used to select the grounding option for the PCIe Bezel. The silk-screen shows AC and DC positions for a shunt to select AC = .1 uF cap to ground , DC = direct connection to ground. No shunt = open connection to ground.

Frequently it is best to DC couple on one side and AC on the other side of a common cable to provide a reference for the cable shield and prevent ground loops.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
The PCI device is mounted to the top edge of PCIe4LBPCI. This can happen before or after installation within the chassis. Hot swap is not supported – the chassis will need to be powered down in either case. It is recommended to screw down the bezel on PCIe4LBPCI to better support the PCI card mounted to it.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId for the PMC installed and an interrupt level. If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. The device manager can be used for Windows OS installations. Linux and other OS generally support alternate PCI listing utilities.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to PCIe4LBPCI when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the PCI installed onto the PCIe4LBPCI than the PCIe4LBPCI itself, and it is smart system design when it can be achieved.

Construction and Reliability

PCIe4LBPCI is constructed out of 0.062 inch thick High Temp FR4 ROHS compliant material. The components on the PCIe4LBPCI are tied into the internal power planes to spread the dissipated heat out over a larger area. This is an effective cooling technique in the situation where a large portion of the board has little or no power dissipation.

Industrial temperate rated surface mounted components are used.

Thermal Considerations

If the PCI installed has large heat dissipation; forced air cooling is recommended for the PCI card and PCIe4LBPCI [depending on chassis air flow].

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
InterNet Address support@dyneng.com

Specifications

Logic Interfaces:	PCI: PCI, PCI-X Interface PCIe: 1-4 lanes
Access types:	PCI bus accesses
CLK rates supported:	133, 100, 66, 50, 33, 25 MHz PCI(x) clock rates
Bus Size Supported:	32 or 64 bit wide operation
Software Interface:	Transparent Bridge. Tsi384 registers in configuration space. Access to registers is usually not required
Initialization:	Dipswitch settings for optimized performance, factory defaults usually best choice, no software required to operate transparent bridge.
Interface:	PCI front bezel via PCI bracket and alternate internal IO via those connectors on PCI device.
Dimensions:	1/2 length PCIe board, single PCIe slot width with PCI installed. Double height with PCI mounted.
Construction:	High Temp ROHS compliant FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.

Order Information

standard temperature range **–40 - 85ºC** rated components

PCIe4LBPCI	4 PCIe lane connector. 1-4 lane operation. Compatible with 4 or more lane backplane connectors. http://www.dyneng.com/PCIe4LBPCI.html [6.595” x 4.194” PCB] PCIe adapter with PCI position Options include: -**ROHS** for ROHS compliant processing -**CC** for conformal coating option -**AP** for PCIe 2x3 added power connector **-JTAG** to add JTAG header to connect to PCI

Step file available with NDA.