



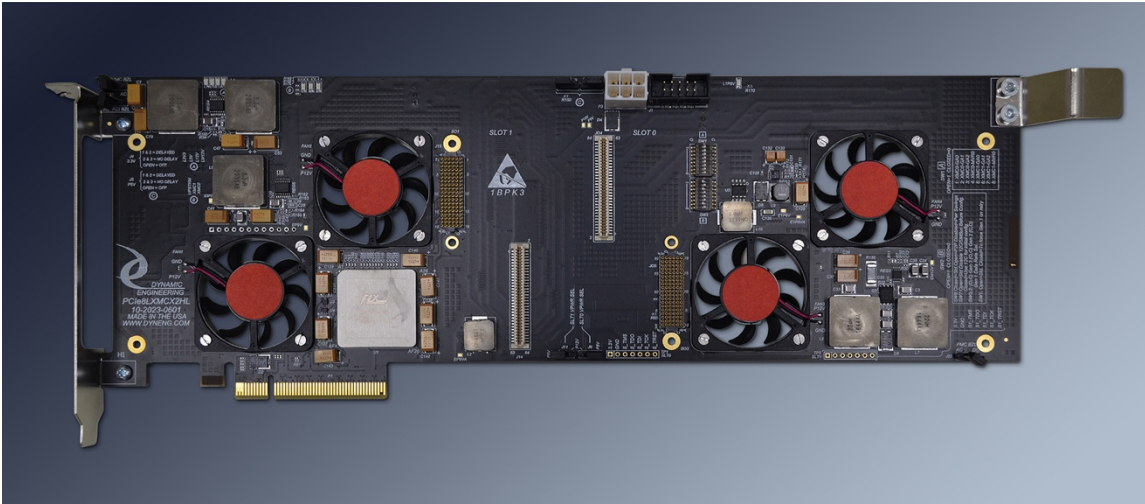
User Manual

PCIe8LXMCX2HL

8-lane, 2-position XMC-Compatible Carrier

Manual Revision	1p0
Revision Date	8/14/23
Corresponding Hardware	(01)
Current Fab Number	10-2023-0601

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PCIe8LXMCX2HL front view with Fans installed

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Cautions and Warnings

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at their own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without express written approval from the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

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Design Revision History

Table 1: Design Revision History

Revision	Date	Description
01	8/14/23	New Design released based on PCIe8LXMCX2 rev 9; altered for customized rear IO connectors.

Manual Revision History

Table 2: Manual Revision History

Revision	Date	Description
1p0	8/14/23	Initial Release

NOTE: Dynamic Engineering has made every effort to ensure that this manual is accurate and complete; that being said, the company reserves the right to make improvements or changes to the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

Product Description

PCIe8LXMCX2HL is part of the Dynamic Engineering PCIe and XMC compatible family of modular I/O components. PCIe8LXMCX2HL adapts two XMCs to one standard PCIe slot. Slots with 8 or more lanes are compatible. PCIe8LXMCX2HL has two XMC card positions. XMC operation Gen1, Gen 2 and Gen 3 PCIe speeds. PCIe8LXMCX2HL can act as a transparent switch, or it can be programmed to allow private operations on the back side (PCIe) bus.

Embedded applications frequently require real-time processing coupled with special purpose I/O. With PCIe8LXMCX2HLs two XMC positions, a PrXMC can be matched with another XMC to make a high bandwidth processing node. The PrXMC can communicate with the host for set-up, and then it can use the local bus to control and transfer data with the special purpose I/O card. With a local processing node of this nature, you can use many cards in parallel with only one computer to provide the system management. For example, 10 in an expansion chassis without overloading the buses or management system.

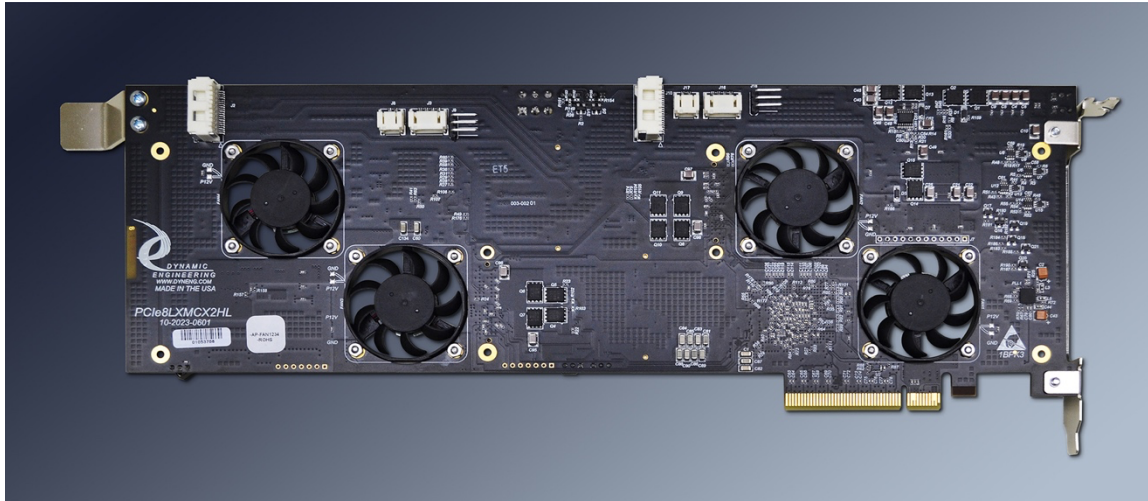
A powerful PCIe 32-lane switch is at the center of the PCIe8LXMCX2HL design. The switch has many capabilities including: operating from 1-8 lanes; operating at Gen1, Gen2, Gen3 or mixed I/O rates; supports lane reversal and polarity inversion (in case your XMC is not working quite right), support for max payload size transfers, fully compliant with the PCIe specification, and more. The switch has 8 PCIe lanes connected to the PCIe gold fingers, and it has 8 connected to each of the XMCs. The PCIe reference clock is buffered with a Gen1-3 compatible clock buffer. The clock buffer is specifically designed to handle spread spectrum and rate locked clocking operation. The buffered clocks are routed to the switch and the two XMC positions. A local power supply and heavy filtering ensure stable power and reliable operation for the switch. The PCIe lanes to and from the switch are routed per PCIe specifications with matched lengths and impedance control.

PCIe8LXMCX2HL is a modified version of PCIe8LXMCX2. The rear IO is customized to route the XMC user I/O connector Pn4 from both positions to client specified connectors. The impedance for the differential signals was also specified at 150 ohms. The XMC front panel connector for slot 1 is mounted through the PCIe mounting bracket. The slot 0 bezel IO [from the XMC] is available at the rear of the card.

For superior performance, PCIe8LXMCX2HL has two cooling cutouts per position that increase airflow to the XMCs. Fan positions are numbered 1-4. Position 1 is closest to the PCIe bezel (left edge of the picture on page ii). Position 2 is closer to the XMC connectors. For positions 3 and 4 continue counting from left to right. One fan can be mounted per position. Fans can be mounted to blow onto the XMC or pull air from the XMC (R option). On PrXMCs and other XMCs with a high thermal load, the fan option is recommended. On cards with lower thermal profile, the fan is not needed. The fan produces 5 CFM in a small area to create a high LFM rating that is suitable for most cooling requirements. See the 'Ordering Information' section for fan and other ordering options.

The PCIe bus does not have a concept of global addressing. A DipSwitch is provided to allow the user to individually select the global address for each of the XMC positions.

PCIe8LXMCX2HL is ready to use with the default settings; simply install the XMC(s) onto the PCIe8LXMCX2HL and then into the system.



Rear view of the HL version of PCIe8LXMCX2. The IO connectors are mounted on this surface to be compatible with the client system. Custom connectors can be added on the front as well.

Key Product Features

Table 3: Key Product Features

Feature	Description
Clocks	Gen1-3 compatible
Voltage Monitors	On +12V, +5V, +12V, -12V Each has an LED that is illuminated when the voltages are within tolerance.
Switch	32-lane, Gen1-3 compliant 8x8x8 configuration with 8 ports not used. Can store and forward locally to communicate directly between the XMCs
Power Supplies	15A - XMC 3.3V 15A – XMC 5V. Shunts for “Delayed”, “Not Delayed”, and “Off” 2A – XMC -12V.
Selection Switch for VPWR	12V or 5V Option for hardwired 5V or 12V
Lanes	8 lanes allocated to PCIe gold finger interface 8 lanes each to the XMCs
Connector access	Front panel connector access through the PCIe bracket
User I/O	Custom connections to client specified connectors with matched length and impedance control.
Cutouts	Allow increased airflow to XMCs Allow option to install fans (see ‘Ordering Information’ section)
JTAG	JTAG programming support XMC JTAG connections are tied to a labeled header. (see ‘Ordering Information’ section)
Global Addressing	Use DipSwitch to select global addressing on XMCs

Product Specifications

Table 4: Product Specifications

Specification	Description
Logic Interfaces	PCIe up to 8 lanes per XMC Gen1-3 compliant switch and clock buffer
Access Type	PCIe TLP transactions MSI interrupts
Clock rates supported	Gen1-3 compatible LEDs show current operating rate – flash rate. DIP switch control to force lower Gen operation etc.
Software Interface	Switch is auto-configured and usually will not require any user intervention
Initialization	Switch selections for VPWR, bezel grounding, and cable options
I/O Interface	Custom connections to client specified connectors with matched length and impedance control.
Dimensions	full-length PCIe board with offset PCIe card guide support
Construction	High-Temp RoHS compliant, FR4 Multi-Layer Printed Circuit, Through Hole, and Surface Mount Components.
Specification Compliance	XMC, PCIe specification compliant

Installation and Interfacing Guidelines

Some general interfacing guidelines are presented below. If you need more assistance, contact Dynamic Engineering.

Installation

Warning: Connection of incompatible hardware is likely to cause serious damage.

The XMCs are mounted to the PCIe8LXMCX2HL prior to installation within the chassis. XMC connectors are rated for 50 insertion cycles, and putting less rotational stress on the connectors is recommended. It is also recommended the PCIe bezel be removed to allow vertical installation on the mating connectors. The rear slot does not have the bezel interaction and can be mounted directly.

NOTE: you can leave the bezel in place and rotate the XMC onto the mating connectors, but this will put some side force on the connectors and is not recommended.

Be careful when removing to restrict the amount of rocking used. Slowly walk the board out of the connector. The connectors are SMT on both sides, and undue stress can fatigue their joints causing premature failure.

There are four mounting locations per XMC: two into the XMC mounting bezel and two for the standoffs near the XMC bus connectors. For proper contact and operation when vibrating, it is recommended that the fasteners are used.

Start-Up

Make sure that the “system” can see your hardware before trying to access it. Many BIOS will display the PCIe devices found at boot up on a “splash screen” with the VendorID and the CardID for the PMC installed and with an interrupt level. If the information is not available from the BIOS, then a third-party PCI device cataloging tool will be helpful. The device manager can be used for Microsoft Windows OS installations.

Guidelines

Grounds – Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should have all their own ground wires back to a common point.

Power Supply – Connecting external voltage to the PCIe8LXMCX2HL when it is not powered, can damage it and the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to XMCs installed onto the PCIe8LXMCX2HL than the PCIe8LXMCX2HL itself, and it is a smart system design when it can be achieved

Thermal Considerations

PCIe8LXMCX2HL has cutouts to support increased airflow over the XMCs component side. On PrXMCs and other XMCs with high thermal loads the fan option is recommended. The zero-slot fan option can provide plenty of cooling power should your XMC require it. On cards with a lower thermal profile, the fan is not needed. The fan produces 5 CFM in a small area to create a high LFM rating suitable for most cooling requirements.

DipSwitch Settings

Switch 1: Global Address settings

Position 1-3: correspond respectively to XMC GA0-2.

When closed, the signal is '0'. When open, the signal is '1'.

Position 4: corresponds to XMC-MVR0.

When closed, the signal is '0'. When open, the signal is '1'.

Position 5-7: correspond to XMC1 GA0-2

When closed, the signal is '0'. When open, the signal is '1'.

Position 8: corresponds to XMC1-MVR0.

When closed, the signal is '0'. When open, the signal is '1'.

The GAO and MVRO signals are optional signals for the XMC not supported by PCIe. SW1 allows the user to set the I2C address for the device and control the Write Inhibit [MVRO] signals.

SW2: Gen 1-3 Switch options

Position 1: Standard = open, Closed = Force Gen1 on retry

Position 3,2 (O,C) = Gen3 (O,O) = Gen2 (C,O) = Gen1 : Data Rate Select

Position 6,5,4 Spare

Position 7 Standard = open => Disable I2C/SMB before configuration

Closed => Use I2C for initial configuration

Position 8 closed P2P is enabled to allow power savings if not used

open P2P is disabled for power savings

Construction and Reliability

PCIe8LXMCX2HL is constructed out of 0.062-inch thick high-temp, RoHS compliant, FR4 material. Cooling cutouts have been designed into the product for improved air flow to the XMC sites. The components of the PCIe8LXMCX2HL are tied into the internal power planes to spread the dissipated heat out over a larger area. This is an effective cooling technique in a situation where a large portion of the board has little or no power dissipation.

A fan option is available for high-thermal load XMCs or for chassis with a lack of air circulation.

Surface Mounted components are used. The connectors are SMT for the XMC bus and Through-Hole for the I/O.

The XMC Module connectors are keyed and shrouded with gold-plated pins on both the plugs and receptacles. They are rated at 1A per pin, 50 insertion cycles. These connectors make consistent, correct insertion easy and reliable.

NOTE: connectors are somewhat delicate compared to PMC and other mezzanine connector types.

The XMC Module is secured against the carrier with the XMC connectors. For enhanced security against temperature and vibration use the XMC mounting screws to retain the device. The screws are supplied with the XMC from the OEM. Dynamic Engineering has screws, standoffs, blank bezels, and other XMC hardware available at a reasonable cost if your XMC was not shipped with some of the required attachment hardware or if it has been misplaced.

Power Supplies

The -12V, 5V, and 3.3V for the XMC are regulated on board. The power supply designs utilize switching regulators controlling MOSFETs to convert 12V to the target voltage. An LC filter ensures clean power at the XMC. The PCIe switch uses a small amount of 3.3, power derived from PCIe 3.3. The PCIe gold fingers are rated for 1.1A each and a total of 5.5A on the +12V rail. 55W are available to the XMCs after power conversion. PCIe8LXMCX2HL has a cable connector to allow an additional 12V of power to be added to the card. The two supplies are DIODE coupled. In some cases, the 12V supply on the backplane will not be adequately routed by the PC causing voltage to sag on the 12V. If this occurs, use the cable connector to compensate.

NOTE: this is the combined power requirement across the +12, -12, +5, and 3.3V power used by the XMCs. In most cases, 55W is sufficient. If not add -AP to the part number to have the Auxiliary Power connector added. 2x3 standard PC connector.

The power supplies include the bulk capacitance to properly bypass the FETs and post conversion voltage rails. Additionally, the XMC connectors are bypassed with a .1uF capacitor at each pin. The power supplies are checked with voltage monitor circuits. The LEDs are not illuminated unless the voltage is within the defined range. Two headers to allow user selection of 5V and 3.3V power on characteristics. The user can use shunts to select “Instant On”, “Delayed On”, or “Disabled.” If your design does not use one of the rails, you can turn it off. If your system enumerates early in the power-up cycle, you can select “Instant On.” If your system can use the delayed setting, load on the power supply can be reduced by spreading out the inrush current.

The XMC specification calls out “VPWR,” which can be either 12V or 5V. PCIe8LXMCX2HL has FET switching and a header to allow user selection of 12V, 5V, or neither voltage to be supplied to these 8 pins (per XMC). The selection is separate per XMC position. Build options are provided to allow “Pre-Selected” voltages on these pins without the headers. The 12V and 5V supplied are part of the same power budget mentioned above. It is suggested that the user select the rail definition that is most efficient for use; alternatively, they can select based on noise. The 5V will likely be quieter since it is converted on board and isolated from the 3.3V rail.

Pinout Options

J6, 11 are used to select the VPWR source for positions 0 and 1 respectively. When the shunt closes 1-2, 12V is selected. With 2-3 closed, 5V is selected. FETs are used to provide a low-impedance path from the power supplies to VPWR for each position. Options are in place on the PCB to allow hardwired selections for clients who prefer a fixed voltage. The headers are not installed when the fixed voltage option is in place. When pin 2 is open, VPWR will be open.

J12, 13, 23 are used to select the bezel grounding option. 1-2 selects AC coupled, 2-3 selects DC coupled, and open is open. J12 = PCIe Bezel. J13 = Slot 0. J23 = Slot 1.

J1 is an optional [2x5] header for SMB connection. Pin 1 is SCL and pin 3 is SDA. Pins 2, 10 are grounded. SCL and SDA are pulled up [4,7K to PCIe 3.3V]. Third party tools can be used to see the “innards” of the switch if the bus is in use. This is usually not needed, and it may be handy if you are doing development or want to access the Switch registers or or talk through the switch to the XMC positions.

TP1, TP2 are optional JTAG headers used to connect to XMC 0 and XMC1 respectively. The pin definitions are in the silk. 1:3.3V, 2:GND, 3:TMS, 4:TDO, 5:TDI, 6:TCK, 7:TRST.

P3 is an optional power connector to allow for added 12V power to be used by the PCIe8LXMCX2HL. The PCIe gold fingers allow for about 60W of power to be consumed by the board across all XMC voltages including power supply losses. In many cases, the power budget is more than sufficient. If your XMCs require more power, please request -AP(2x3 standard PC power connector) to increase the 12V available. Both 12V entry points are diode coupled to prevent the current back-feeding when an external or other supply is added.

P3: 1-3 = 12V, 4-6 = ground

13A per pin is the rating on the connector. 12A limited by diode.

J4, 5 control the power sequencing for 3.3V and 5V respectively. 1-2 selects a delayed startup of the power supply. 2-3 selects immediate startup (based on 12V being available). Open is off (used for power savings when a supply is not required). Added with revision 03 boards. Resistor options are available to hardwire the selection.

Pin Assignments

XMC Module Backplane I/O Interface

The figure below gives the pin assignments for the XMC Module I/O Interface from Jn4 and/or Jn6 to the PCIe8LXMCX2 connectors. See the User Manual for the XMC board being used for more information.

NOTE: P2 and P13, P7 and P5 have dual footprints, only one of each pair can be installed.

Table 5: XMC Module Rear I/O Interface Pin Assignments

J2/J10	J3/J16	J8/J17	J9/J18	Jn4	
			1 /	3	1
				4	2
			/ 3	7	5
	1 /	1 /		8	6
				11	9
	2,3 / 4	2 /		12	10
				15	13
				16	14
				19	17
				20	18
				23	21
				24	22
				27	25
				28	26
				31	29
				32	30
3 / 4				35	33
1 / 2				36	34
				39	37
				40	38
				43	41
				44	42
				47	45
				48	46
				51	49
				52	50
9 / 10				55	53
7 / 8				56	54
13 / 14				59	57
11 / 12				60	58
19 / 20				63	61
17 / 18				64	62

Read table: sides of / to see which column of Jn4 to use

Pin1 of J2 & J10 are tied to J04.36 & J14.36 respectively With J2.2 & J10.2 tied to J04.34 & J14.34

Grounded pins: J2, J10 pins 5,6,15,16 J9,J18 pin 2

J2, J10 are routed with 150 ohm differential matched length

The remaining signals are 50 ohms with similar lengths.

Warranty and Repair

Please refer to the warranty page on our website for the warranty and options that are currently offered.

www.dyneng.com/warranty

Service Policy

Before returning a product for repair, verify to the best of your ability, that the suspected unit is as fault. Then call the Dynamic Engineering Customer Service Department for a Return Material Authorization (RMA) number. Carefully package the product, in the original packaging if possible, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by anyone other than the original customer will be treated as out-of-warranty.

Out-of-Warranty Repairs

Out-of-warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the list price for one of that kind of unit. Return transportation and insurance will be billed as part of the repair in addition to the minimum RMA charge.

Contact:

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Ordering Information

Standard Temperature Range-Rated Components: -40 - 85°C

Table 6: Ordering Information

Product	Description	
PCIe8LXMCX2HL	Full length PCIe design with two XMC positions, Custom Connectors, User VPWR selection, and standard (non-RoHS) solder and components. www.dyneng.com/PCIe8LXMCX2HL	
	Options:	
	-Fan_	Fan1 for position 1; Fan2 for position 2; Fan3 for position 3; Fan4 for position 4; Fan1234 for all positions Low profile fans Push air toward the XMC
	-Fan_Rz	Fan1Rz; Fan2Rz; Fan3Rz; Fan4Rz; Fan1Rz2Rz Rear mount low-profile fans Pull air away from the XMC
	-Fan_R	Fan1R; Fan2R; Fan3R; Fan4R; Fan1R2R3R4R 8 CFM fan Only available as rear mount Pull air away from the XMC
	-RoHS	Use RoHS processing. Standard processing is "leaded."
	-CC	Option to add conformal coating
	-5VXXX	5V supply forced to (replace XXX). No Delay [ND], Delay [DEL], off [OFF] instead of user selectable
	-3VXXX	3V supply forced to (replace XXX). No Delay [ND], Delay [DEL], off [OFF] instead of user selectable
	-VPWR5V	VPWR forced to 5V instead of user selectable
	-VPWR12V	VPWR forced to 12V instead of user selectable
	-AP	Add 2x3 PC style Power connector for supplemental Power

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Glossary

Baud	Used as the bit period when talking about UARTs; Not strictly correct, but is the common usage when talking about UARTs.
CardID	Unique number assigned to a design to distinguish between all designs of a particular vendor
CFM	Cubic feet per minute
FIFO	First In First Out memory
Flash	Non-volatile memory used on Dynamic Engineering boards to store FPGA configurations or BIOS
JTAG	Joint Test Action Group – a standard used to control serial data transfer for test and programming operations.
LFM	Linear feet per minute
MUX	Multiplexor – multiple signals multiplexed to one with a selection mechanism to control which path is active.
Packed	When UART characters are always sent/received in groups of four, allowing full use of host bus/FIFO bandwidth.
Packet	Group of characters transferred. When the characteristics of the group of characters is known, the data can be stored in packets and transferred as such; the system is optimized as a result. Any number of characters can be transferred.
PCI	Peripheral Component Interconnect – parallel bus from host to this device
PMC	PCI Mezzanine Card – establishes common connectors, connections, size and other mechanical features.
TAP	Test Access Port – basically a multi-state port that can be controlled with JTAG [TMS, TDI, TDO, TCK]. The TAP States are the states in the State Machine that are controlled by the commands received over the JTAG link.
TCK	Test Clock provides synchronization for the TDI, TDO, and TMS signals
TDI	Test Data in – this serial line provides the data input to the device controlled by the TMS commands. For example, the data to program the FLASH comes on the TDI line while the commands to the state machine to move through the necessary states comes over TMS. Rising edge of TCK valid.
TDO	Test Data Out is the shifted data out. Valid on the falling edge of the TCK. Not all states output data.

TMS	Test Mode State – this serial line provides the state switching controls. ‘1’ indicates to move to the next state, ‘0’ means stay put in cases where delays can happen; otherwise, 0,2 are used to choose which branch to take. Due to the complexity of state manipulation, the instructions are usually precompiled. Rising edge of TCK valid.
UART	Universal Asynchronous Receiver Transmitter. Common serialized data transfer with start bit, stop bit, optional parity, optional 7/8 bit data. Can be over any electrical interface. RS232 and RS422 are most common.
Unpacked	When UART characters are sent on an unknown basis requiring single character storage and transfer over the host bus
VendorID	Manufacturers number for PCI/PCIe boards. DCBA is Dynamic Engineering’s VendorID