User Manual

PCIe8LXMCX2

8-lane, 2-position XMC-Compatible Carrier

Manual Revision	6p4
Revision Date	04/25/25
Corresponding Hardware	(09-13)
Current Fab Number	10-2012-0113

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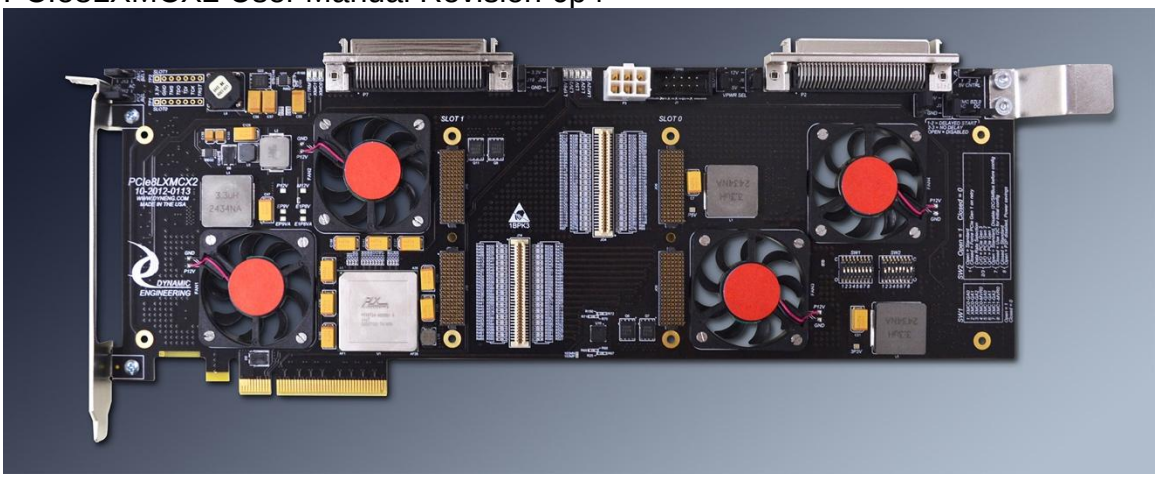

PCIe8LXMCX2 with Fans installed rev 13 shown

Cautions and Warnings

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at their own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without express written approval from the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

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Design Revision History

Table 1: Design Revision History

Revision	Date	Description
NOTE: Revision history may be incomplete for boards released prior to 7/31/2020		
A	1/2/2012	New Design released based on PCIeBPMCX2; altered for XMC
B	5/2/2012	Updated for blocking caps and misc. settings to improve switch operation
C	7/18/2012	Fab-only update for slight interference at PCIe gold fingers
D	10/3/2013	Added option for XMC [Pn6]
E	4/23/2015	Switched to 0402 resistors, updated some footprints, added option for removing start-up delay
F	2/3/2016	Corrected 1V LED name
07	2/28/2019	Updated caps for larger M12V capability, and updated 5V and 3.3V to 15A
08		Add JTAG support to second position
09	11/23/22	Update design to use Gen3 switch and incorporate CB option. Remove Enet and Ser options.
10	12/7/23	Manufacturing updates to PCB
11	10/31/23	Update for EOL inductor
12	7/11/24	Not built
13	12/10/24	Manufacturing and routing updates, minor part changes

Manual Revision History

Table 2: Manual Revision History

Revision	Date	Description
NOTE: Revision history may be incomplete for revisions prior to 7/31/2020		
B1	10/1/2012	Corresponds to board revision B/C for 10-2012-010(2,3)
D1	10/30/2015	Corresponds to board revision C/D for 10-2012-010(3,4) Updated to reflect changes made when board was updated
E1	6/28/2016	Corresponds to board revision C/D/E for 10-2012-010(3-5) Updated to reflect changes made when board was updated
E2	8/29/2016	Corresponds to board revision C/D/E for 10-2012-010(3-5) Added J4 and J5 pinout options (applicable to Rev 3 and later boards) Updated 'Ordering Information' section
E3	12/28/2017	Corresponds to board revision C-F for 10-2012-010(3-6) Updated to reflect changes made when board was updated
05p4	7/31/2020	Corresponds to board revision C-F for 10-2012-010(3-6) Updated formatting to increase clarity and ease of use
6p0 6p1 6p2 6p3 6p4	11/23/22 12/7/22 12/7/23 3/5/25 4/25/25	Corresponds to Rev 09. 10-2012-09 and later. Add missing SW2 description Add errata for revision 10 Corresponds to Rev 13 10-2012-0113 and later Add missing information about LEDs

NOTE: Dynamic Engineering has made every effort to ensure that this manual is accurate and complete; that being said, the company reserves the right to make improvements or changes to the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

Product Description

PCIe8LXMCX2 is part of the Dynamic Engineering PCIe and XMC compatible family of modular I/O components. PCIe8LXMCX2 adapts two XMCs to one standard PCIe slot. Slots with 8 or more lanes are compatible. PCIe8LXMCX2 has two XMC card positions. XMC operation Gen1, Gen 2 and Gen 3 PCIe speeds. PCIe8LXMCX2 can act as a transparent switch, or it can be programmed to allow private operations on the back side (PCIe) bus.

Embedded applications frequently require real-time processing coupled with special purpose I/O. With the two PCIe8LXMCX2 XMC positions, a PrXMC can be matched with another XMC to make a high bandwidth processing node. The PrXMC can communicate with the host for set-up, and then it can use the local bus to control and transfer data with the special purpose I/O card. With a local processing node of this nature, you can use many cards in parallel with only one computer to provide the system management. For example, 10 in an expansion chassis without overloading the buses or management system.

A powerful PCIe 32-lane switch is at the center of the PCIe8LXMCX2 design. The switch has many capabilities including: operating from 1-8 lanes; operating at Gen1, Gen2, Gen3 or mixed I/O rates; supports lane reversal and polarity inversion (in case your XMC is not working quite right), support for max payload size transfers, fully compliant with the PCIe specification, and more. The switch has 8 PCIe lanes connected to the PCIe gold fingers, and it has 8 connected to each of the XMCs. The PCIe reference clock is buffered with a Gen1-3 compatible clock buffer. The clock buffer is specifically designed to handle spread spectrum and rate locked clocking operation. The buffered clocks are routed to the switch and the two XMC positions. A local power supply and heavy filtering ensure stable power and reliable operation for the switch. The PCIe lanes to and from the switch are routed per PCIe specifications with matched lengths and impedance control.

XMC user I/O connector Pn4 or Pn6 from both positions is brought out to SCSI connectors. The signals are isolated with resistors to keep the routing short and to allow for the Connector Bus option. The XMC front panel connector for slot 1 is mounted through the PCIe mounting bracket.

For superior performance, PCIe8LXMCX2 has two cooling cutouts per position that increase airflow to the XMCs. Fan positions are numbered 1-4. Position 1 is closest to the PCIe bezel (left edge of the picture on page ii). Position 2 is closer to the XMC connectors. For positions 3 and 4 continue counting from left to right. One fan can be mounted per position. Fans can be mounted to blow onto the XMC or pull air from the

XMC (R option). On PrXMCs and other XMCs with a high thermal load, the fan option is recommended. On cards with lower thermal profile, the fan is not needed. The fan produces 5 CFM in a small area to create a high LFM rating that is suitable for most cooling requirements. See the 'Ordering Information' section for fan and other ordering options.

The PCIe bus does not have a concept of global addressing. A DipSwitch is provided to allow the user to individually select the global address for each of the XMC positions.

The individual pins on the Jn4 (Pn4) and Jn6 (Pn6) connectors for each position can be interconnected [-CB] and/or routed to the 68-pin SCSI connector. The I/O are routed with matched-length, impedance-controlled differential traces suitable for single-ended and differential operation. Normally with the **C**onnector **B**us option the SCSI connectors are not populated. 0 ohm resistors are used to isolate the options and provide "no stub" connections for the CB and IO options.

The -CB option is used to provide a high-speed interconnect between the two installed XMCs. The interconnect is direct without a switch or other delaying logic in the path. This option previously was available on a separate PCB. The feature has been incorporated into the base design. For partial allocations – some CB and some IO please contact Dynamic Engineering. We can assign a new option to install the corresponding isolation resistors.

Dynamic Engineering recommends using their SCSI cable and HDEterm68 breakout block with the SCSI connector. The industry standard VME IDC (DIN) connector is easy to connect to your system using DINterm64, a 64-position terminal strip, and the DINribn64, a 64-position ribbon cable.

Additionally, PCIe8LXMCX2 has two options for Jn4/Jn6 signal routing. The default is Jn4/Pn4 signal path. -XIO adds the Jn6/Pn6 connector path. -XIOexc provides the Jn4/Pn6 signal path exclusively.

Cables and breakouts are available from Dynamic Engineering. Please see the 'Ordering Information' section of this manual for more information on HDEcabl68, and HDEterm68.

PCIe8LXMCX2 is ready to use with the default settings; simply install the XMC(s) onto the PCIe8LXMCX2 and then into the system.

Key Product Features

Table 3: Key Product Features

Feature	Description
Clocks	Gen1-3 compatible
Voltage Monitors	On +12V, +5V, +12V, -12V Each has an LED that is illuminated when the voltages are within tolerance.
Switch	32-lane, Gen1-3 compliant 8x8x8 configuration with 8 ports not used. Can store and forward locally to communicate directly between the XMCs
Power Supplies	15A - XMC 3.3V 15A – XMC 5V. Shunts for “Delayed”, “Not Delayed”, and “Off” 2A – XMC -12V.
Selection Switch for VPWR	12V or 5V Option for hardwired 5V or 12V
Lanes	8 lanes allocated to PCIe gold finger interface 8 lanes each to the XMCs
Connector access	Front panel connector access through the PCIe bracket
User I/O	Jn4 and/or Jn6 Available through one of two cable connectors: SCSI II Spare pins on SCSI connector can be shunt selected to power or ground. Option to cross connect Rear IO connectors.
Cutouts	Allow increased airflow to XMCs Allow option to install fans (see ‘Ordering Information’ section)
JTAG	JTAG programming support XMC JTAG connections are tied to a labeled header. (see ‘Ordering Information’ section)
Global Addressing	Use DipSwitch to select global addressing on XMCs

Product Specifications

Table 4: Product Specifications

Specification	Description
Logic Interfaces	PCIe up to 8 lanes per XMC Gen1-3 compliant switch and clock buffer
Access Type	PCIe TLP transactions MSI interrupts
Clock rates supported	Gen1-3 compatible LEDs show current operating rate – flash rate. DIP switch control to force lower Gen operation etc.
Software Interface	Switch is auto-configured and usually will not require any user intervention
Initialization	Switch selections for VPWR, bezel grounding, and cable options
I/O Interface	XMC bezel I/O supported at PCIe bracket Jn4/Jn6 “user I/O” supported with SCSI connectors at both positions Connector Bus option to cross connect XMC0 & XMC1 Rear IO.
Dimensions	full-length PCIe board with offset PCIe card guide support
Construction	High-Temp RoHS compliant, FR4 Multi-Layer Printed Circuit, Through Hole, and Surface Mount Components.
Specification Compliance	XMC, PCIe specification compliant

Installation and Interfacing Guidelines

Some general interfacing guidelines are presented below. If you need more assistance, contact Dynamic Engineering.

Installation

Warning: Connection of incompatible hardware is likely to cause serious damage.

The XMCs are mounted to the PCIe8LXMCX2 prior to installation within the chassis. XMC connectors are rated for 50 insertion cycles, and putting less rotational stress on the connectors is recommended. It is also recommended the PCIe bezel be removed to allow vertical installation on the mating connectors. The rear slot does not have the bezel interaction and can be mounted directly.

NOTE: you can leave the bezel in place and rotate the XMC onto the mating connectors, but this will put some side force on the connectors and is not recommended.

Be careful when removing to restrict the amount of rocking used. Slowly walk the board out of the connector. The connectors are SMT on both sides, and undue stress can fatigue their joints causing premature failure.

There are four mounting locations per XMC: two into the XMC mounting bezel and two for the standoffs near the XMC bus connectors. For proper contact and operation when vibrating, it is recommended that the fasteners are used.

Start-Up

Make sure that the “system” can see your hardware before trying to access it. Many BIOS will display the PCIe devices found at boot up on a “splash screen” with the VendorID and the CardID for the PMC installed and with an interrupt level. If the information is not available from the BIOS, then a third-party PCI device cataloging tool will be helpful. The device manager can be used for Microsoft Windows OS installations.

Guidelines

Grounds – Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should have all their own ground wires back to a common point.

Power Supply – Connecting external voltage to the PCIe8LXMCX2 when it is not powered, can damage it and the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to XMCs installed onto the PCIe8LXMCX2 than the PCIe8LXMCX2 itself, and it is a smart system design when it can be achieved

Thermal Considerations

PCIe8LXMCX2 has cutouts to support increased airflow over the XMCs component side. On PrXMCs and other XMCs with high thermal loads the fan option is recommended. The zero-slot fan option can provide plenty of cooling power should your XMC require it. On cards with a lower thermal profile, the fan is not needed. FANs produce 5 CFM concentrated for a high LFM rating suitable for most requirements.

DipSwitch Settings

Switch 1: Global Address settings

Position 1-3: correspond respectively to XMC GA0-2.

When closed, the signal is ‘0’. When open, the signal is ‘1’.

Position 4: corresponds to XMC-MVR0.

When closed, the signal is ‘0’. When open, the signal is ‘1’.

Position 5-7: correspond to XMC1 GA0-2

When closed, the signal is ‘0’. When open, the signal is ‘1’.

Position 8: corresponds to XMC1-MVR0.

When closed, the signal is ‘0’. When open, the signal is ‘1’.

The GAO and MVRO signals are optional signals for the XMC not supported by PCIe. SW1 allows the user to set the I2C address for the device and control the Write Inhibit [MVRO] signals.

SW2: Gen 1-3 Switch options
Position 1: Standard = open, Closed = Force Gen1 on retry
Position 3,2 (O,C) = Gen3 (O,O) = Gen2 (C,O) = Gen1 : Data Rate Select
Position 6,5,4 Spare
Position 7 Standard = open => Disable I2C/SMB before configuration
Closed => Use I2C for initial configuration

Position 8 closed P2P is enabled to allow power savings if not used
open P2P is disabled for power savings

LEDs

Upstream, XMC0, XMC1 are located above the left edge of Fan position 2. The LEDs are illuminated when the link is in operation. Upstream = link between host and switch. XMC0 and XMC1 are the respective links between the switch and XMC devices.

Steady on corresponds to G3 speed. Blinking 256 mS on-off is G2. 512 mS on-off is G1.

L1P8 is illuminated when the 1.8V power supply is within tolerance. Sourced from 12V system supply.

L12V is illuminated when the 12V rail from the system is within tolerance. If this LED is off or flashing check the power supply capability. You may need a larger supply or to add the -AP option and a secondary power cable.

LM12V is illuminated when the -12V rail from the system is within tolerance. Local power supply based on P12V rail.

L5V is illuminated when the 5V power supply is within tolerance. Sourced from 12V system supply.

L3V3 is illuminated when the 3.3V power supply is within tolerance. Sourced from 12V system supply.

Construction and Reliability

PCIe8LXMCX2 is constructed out of 0.062-inch thick high-temp, RoHS compliant, FR4 material. Cooling cutouts have been designed into the product for improved air flow to the XMC sites. The components of the PCIe8LXMCX2 are tied into the internal power planes to spread the dissipated heat out over a larger area. This is an effective cooling technique in a situation where a large portion of the board has little or no power dissipation.

A fan option is available for high-thermal load XMCs or for chassis with a lack of air circulation.

Surface Mounted components are used. The connectors are SMT for the XMC bus and Through-Hole for the I/O.

The XMC Module connectors are keyed and shrouded with gold-plated pins on both the plugs and receptacles. They are rated at 1A per pin, 50 insertion cycles. These connectors make consistent, correct insertion easy and reliable.

NOTE: connectors are somewhat delicate compared to PMC and other mezzanine connector types.

The XMC Module is secured against the carrier with the XMC connectors. For enhanced security against temperature and vibration use the XMC mounting screws to retain the device. The screws are supplied with the XMC from the OEM. Dynamic Engineering has screws, standoffs, blank bezels, and other XMC hardware available at a reasonable cost if your XMC was not shipped with some of the required attachment hardware or if it has been misplaced.

Power Supplies

The -12V, 5V, and 3.3V for the XMC are regulated on board. The power supply designs utilize switching regulators controlling MOSFETs to convert 12V to the target voltage. An LC filter ensures clean power at the XMC. The PCIe switch uses a small amount of 3.3, power derived from PCIe 3.3. The PCIe gold fingers are rated for 1.1A each and a total of 5.5A on the +12V rail. 55W are available to the XMCs after power conversion. PCIe8LXMCX2 has a cable connector to allow an additional 12V of power to be added to the card. The two supplies are DIODE coupled. In some cases, the 12V supply on the backplane will not be adequately routed by the PC causing voltage to sag on the 12V. If this occurs, use the cable connector to compensate.

NOTE: this is the combined power requirement across the +12, -12, +5, and 3.3V power used by the XMCs. In most cases, 55W is sufficient. If not add -AP to the part number to have the Auxiliary Power connector added. 2x3 standard PC connector.

The power supplies include the bulk capacitance to properly bypass the FETs and post conversion voltage rails. Additionally, the XMC connectors are bypassed with a .1uF capacitor at each pin. The power supplies are checked with voltage monitor circuits. The LEDs are not illuminated unless the voltage is within the defined range.

A header is used to select 5V power on characteristics. The user can use a shunt to select “Instant On”, “Delayed On”, or “Disabled.” If your design does not use 5V, you can turn it off. If your system enumerates early in the power-up cycle, you can select “Instant On.” If your system can use the delayed setting, load on the power supply can be reduced by spreading out the inrush current.

The XMC specification calls out “VPWR,” which can be either 12V or 5V. PCIe8LXMCX2 has FET switching and a header to allow user selection of 12V, 5V, or neither voltage to be supplied to these 8 pins (per XMC). The selection is separate per XMC position. Build options are provided to allow “Pre-Selected” voltages on these pins without the headers. The 12V and 5V supplied are part of the same power budget mentioned above. It is suggested that the user select the rail definition that is most efficient for use; alternatively, they can select based on noise. The 5V will likely be quieter since it is converted on board and isolated from the 3.3V rail.

Pinout Options

J6, 11 are used to select the VPWR source for positions 0 and 1 respectively. When the shunt closes 1-2, 12V is selected. With 2-3 closed, 5V is selected. FETs are used to provide a low-impedance path from the power supplies to VPWR for each position. Options are in place on the PCB to allow hardwired selections for clients who prefer a fixed voltage. The headers are not installed when the fixed voltage option is in place. When pin 2 is open, VPWR will be open.

J12, 13, 23 are used to select the bezel grounding option. 1-2 selects AC coupled, 2-3 selects DC coupled, and open is open. J12 = PCIe Bezel. J13 = Slot 0. J23 = Slot 1.

J1 is an optional [2x5] header for SMB connection. Pin 1 is SCL and pin 3 is SDA. Pins 2, 10 are grounded. SCL and SDA are pulled up [4,7K to PCIe 3.3V]. Third party tools can be used to see the “innards” of the switch if the bus is in use. This is usually not needed, and it may be handy if you are doing development or want to access the Switch registers or or talk through the switch to the XMC positions.

TP1, TP2 are optional JTAG header used to connect to XMC 0 and XMC1 respectively. The pin definitions are in the silk. 1:3.3V, 2:GND, 3:TMS, 4:TDO, 5:TDI, 6:TCK, 7:TRST.

J2, 3 control the voltage on 33,67 of P2 when the SCSI connector options are selected. 1-2 selects 3.3V. 2-3 selects ground. The shunt and traces are rated for 1A. Not fuse protected

J19, 20 control the voltage on 34,68 of P7 when the SCSI connector options are selected. 1-2 selects 3.3V. 2-3 selects ground. The shunt and traces are rated for 1A. Not fuse protected

P3 is an optional power connector to allow for added 12V power to be used by the PCIe8LXMCX2. The PCIe gold fingers allow for about 60W of power to be consumed by the board across all XMC voltages including power supply losses. In many cases, the power budget is more than sufficient. If your XMCs require more power, please request -AP(2x3 standard PC power connector) to increase the 12V available. Both 12V entry points are diode coupled to prevent the current back-feeding when an external or other supply is added.

P3: 1-3 = 12V, 4-6 = ground
13A per pin is the rating on the connector. 12A limited by diode.

J5 controls the turn on delay for the 5V power supply. 1-2 selects a delayed startup of the power supply. 2-3 selects immediate startup (based on 12V being available). Open is off (used for power savings when a supply is not required). Added with revision 03 boards. Resistor options are available to hardwire the selection.

Pin Assignments

XMC Module Backplane I/O Interface

The figure below gives the pin assignments for the XMC Module I/O Interface from Jn4 and/or Jn6 to the PCIe8LXMCX2 connectors. See the User Manual for the XMC board being used for more information.

NOTE: P2 and P13, P7 and P5 have dual footprints, only one of each pair can be installed.

Table 5: XMC Module Backplane I/O Interface Pin Assignments

DIN IDC [P13, P5]		SCSI II [P2, P7]		Jn4		Jn6	
A1	C1	1	35	3	1	B1	A1
A2	C2	2	36	4	2	E1	D1
A3	C3	3	37	7	5	C2	C1
A4	C4	4	38	8	6	F2	F1
A5	C5	5	39	11	9	B3	A3
A6	C6	6	40	12	10	E3	D3
A7	C7	7	41	15	13	C4	C3
A8	C8	8	42	16	14	F4	F3
A9	C9	9	43	19	17	B5	A5
A10	C10	10	44	20	18	E5	D5
A11	C11	11	45	23	21	C6	C5
A12	C12	12	46	24	22	F6	F5
A13	C13	13	47	27	25	B7	A7
A14	C14	14	48	28	26	E7	D7
A15	C15	15	49	31	29	C8	C7
A16	C16	16	50	32	30	F8	F7
A17	C17	17	51	35	33	B9	A9
A18	C18	18	52	36	34	E9	D9
A19	C19	19	53	39	37	C10	C9
A20	C20	20	54	40	38	F10	F9
A21	C21	21	55	43	41	B11	A11
A22	C22	22	56	44	42	E11	D11
A23	C23	23	57	47	45	C12	C11
A24	C24	24	58	48	46	F12	F11
A25	C25	25	59	51	49	B13	A13
A26	C26	26	60	52	50	E13	D13
A27	C27	27	61	55	53	B15	A15
A28	C28	28	62	56	54	E15	D15
A29	C29	29	63	59	57	B17	A17
A30	C30	30	64	60	58	E17	D17
A31	C31	31	65	63	61	B19	A19
A32	C32	32	66	64	62	E19	D19
		33	67	Open, +3 or GND via J2,19 silk screen defined			
		34	68	Open, +3 or GND via J3,20			

Read table: P12-C1 = P2-35 = Jn4-1

P13-A1 = P2-1 = Jn4-3 etc.

With Jn6, pins: A, B, D, E of rows 2, 4, 6, 8, 10, 12, 14, 16, & 18 are grounded

Warranty and Repair

Please refer to the warranty page on our website for the warranty and options that are currently offered.

www.dyneng.com/warranty

Service Policy

Before returning a product for repair, verify to the best of your ability, that the suspected unit is as fault. Then call the Dynamic Engineering Customer Service Department for a Return Material Authorization (RMA) number. Carefully package the product, in the original packaging if possible, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by anyone other than the original customer will be treated as out-of-warranty.

Out-of-Warranty Repairs

Out-of-warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the list price for one of that kind of unit. Return transportation and insurance will be billed as part of the repair in addition to the minimum RMA charge.

Contact:

Customer Service Department

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Ordering Information

Standard Temperature Range-Rated Components: -40 - 85°C

Table 6: Ordering Information

Product	Description	
PCIe8LXMCX2	Full length PCIe design with two XMC positions, SCSI connectors installed, User VPWR selection, and standard (non-RoHS) solder and components. www.dyneng.com/PCIe8LXMCX2 Options:	
	-Fan_	Fan1 for position 1; Fan2 for position 2; Fan3 for position 3; Fan4 for position 4; Fan1234 for all positions Low profile fans Push air toward the XMC
	-Fan_Rz	Fan1Rz; Fan2Rz; Fan3Rz; Fan4Rz; Fan1Rz2Rz Rear mount low-profile fans Pull air away from the XMC
	-Fan_R	Fan1R; Fan2R; Fan3R; Fan4R; Fan1R2R3R4R 8 CFM fan Only available as rear mount Pull air away from the XMC
	-SCSI	SCSI connector installed – also the default selection
	-NC	No SCSI connector installed
	-RoHS	Use RoHS processing. Standard processing is “leaded.”
	-CC	Option to add conformal coating
	-5VXXX	5V supply forced to (replace XXX). No Delay [ND], Delay [DEL], off [OFF] instead of user selectable
	-XIO	Board comes with both Jn4 and Jn6 installed
	-XIOExc	Board comes with only Jn6 installed (no Jn4)
	-VPWR5V	VPWR forced to 5V instead of user selectable
	-VPWR12V	VPWR forced to 12V instead of user selectable
	-CB	Connector Bus option to interconnect the rear IO connectors. Matched length, differential, impedance controlled routing. Resistor isolation to remove bus stubs from other options.
	-AP	Add 2x3 PC style Power connector for supplemental Power

HDEterm68	68-pin SCSI II to 68 screw terminal adapter with DIN rail mounting www.dyneng.com/HDEterm68
HDEcabl68	SCSI cables with latch blocks or thumbscrews. Various lengths available. Custom lengths can be ordered. www.dyneng.com/HDEcabl68
DINribn64	64-pin ribbon cable with strain relief. Add -XX for number of inches. 36-inch is the default. www.dyneng.com/DINribn64

Glossary

Baud	Used as the bit period when talking about UARTs; Not strictly correct, but is the common usage when talking about UARTs.
CardID	Unique number assigned to a design to distinguish between all designs of a particular vendor
CFM	Cubic feet per minute
FIFO	First In First Out memory
Flash	Non-volatile memory used on Dynamic Engineering boards to store FPGA configurations or BIOS
JTAG	Joint Test Action Group – a standard used to control serial data transfer for test and programming operations.
LFM	Linear feet per minute
MUX	Multiplexor – multiple signals multiplexed to one with a selection mechanism to control which path is active.
Packed	When UART characters are always sent/received in groups of four, allowing full use of host bus/FIFO bandwidth.
Packet	Group of characters transferred. When the characteristics of the group of characters is known, the data can be stored in packets and transferred as such; the system is optimized as a result. Any number of characters can be transferred.
PCI	Peripheral Component Interconnect – parallel bus from host to this device
PMC	PCI Mezzanine Card – establishes common connectors, connections, size and other mechanical features.
TAP	Test Access Port – basically a multi-state port that can be controlled with JTAG [TMS, TDI, TDO, TCK]. The TAP States are the states in the State Machine that are controlled by the commands received over the JTAG link.
TCK	Test Clock provides synchronization for the TDI, TDO, and TMS signals
TDI	Test Data in – this serial line provides the data input to the device controlled by the TMS commands. For example, the data to program the FLASH comes on the TDI line while the commands to the state machine to move through the necessary states comes over TMS. Rising edge of TCK valid.
TDO	Test Data Out is the shifted data out. Valid on the falling edge of the TCK. Not all states output data.

TMS	Test Mode State – this serial line provides the state switching controls. ‘1’ indicates to move to the next state, ‘0’ means stay put in cases where delays can happen; otherwise, 0,2 are used to choose which branch to take. Due to the complexity of state manipulation, the instructions are usually precompiled. Rising edge of TCK valid.
UART	Universal Asynchronous Receiver Transmitter. Common serialized data transfer with start bit, stop bit, optional parity, optional 7/8 bit data. Can be over any electrical interface. RS232 and RS422 are most common.
Unpacked	When UART characters are sent on an unknown basis requiring single character storage and transfer over the host bus
VendorID	Manufacturers number for PCI/PCIe boards. DCBA is Dynamic Engineering’s VendorID