User Manual

PCIeNLXMCX1

XMC-Compatible Carriers

Manual Revision 04p3
Revision Date 07/12/23

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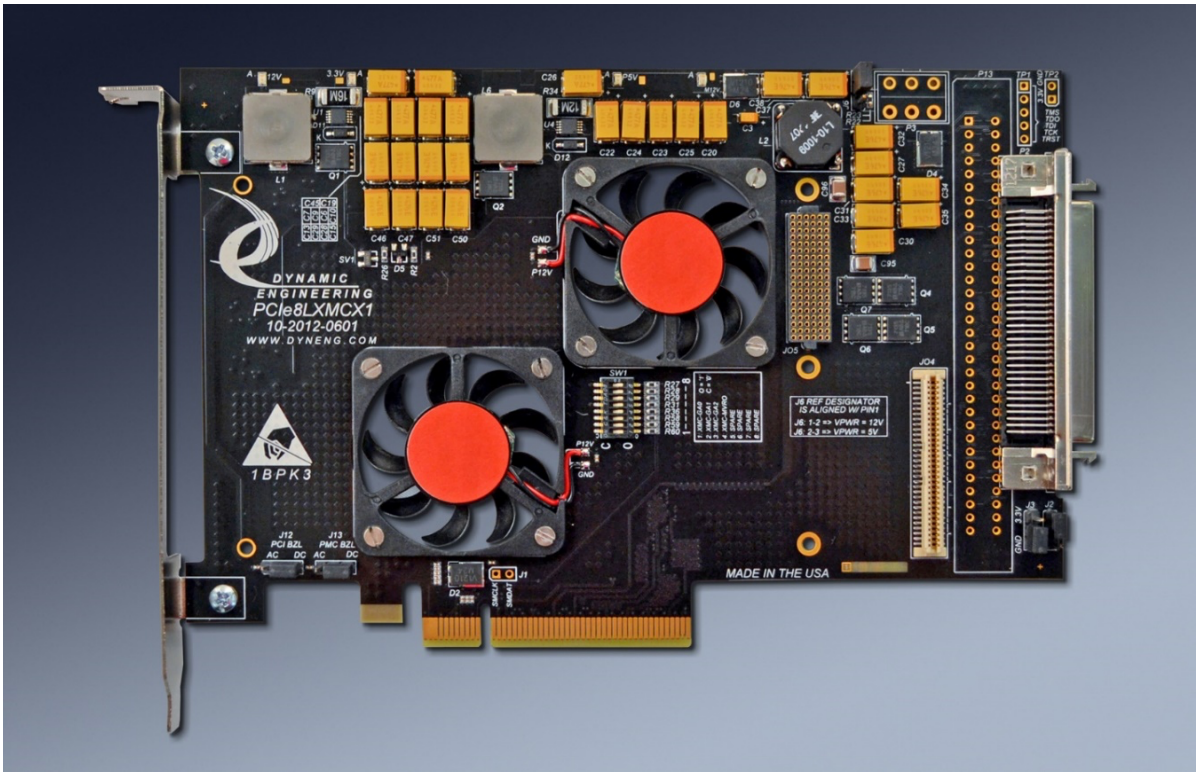
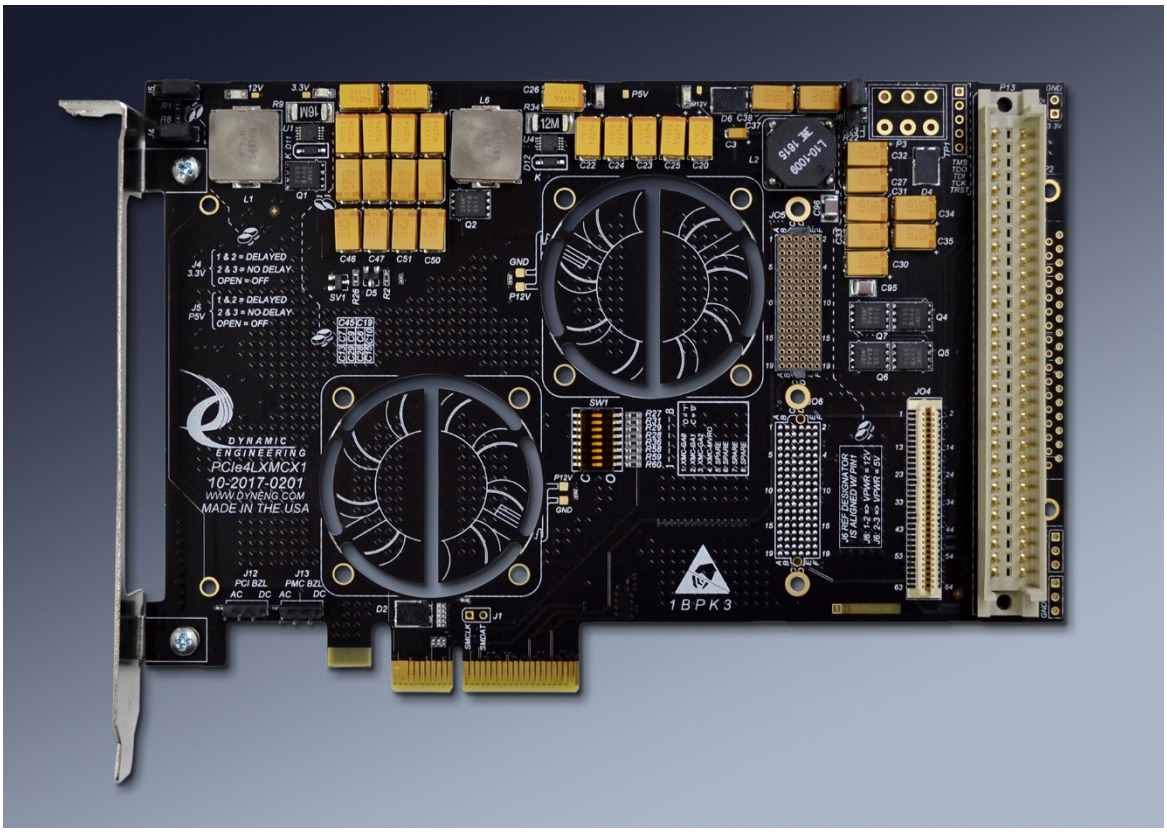
PCIe8LXMCX1: an 8-Lane, XMC-Compatible Carrier



Corresponding Hardware: 10-2012-060(7,8)

PCIe4LXMCX1: a 4-Lane, XMC-Compatible Carrier



Corresponding Hardware: 10-2017-010(1&2)

Cautions and Warnings

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at their own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without express written approval from the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

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Tables

Design Revision History

Table 1: Design Revision History

Revision	Date	Description
Rev A PCIe8LXMCX1	6/19/2012	Initial release of the PCIe8LXMCX1 Based on PCIe8LXMCX2, altered for single position
Rev B PCIe8LXMCX1	5/17/2013	Updated layout for better connector positioning
Rev C PCIe8LXMCX1	5/14/2015	Added XIO option and power sequencing user selections
Rev D PCIe8LXMCX1	3/19/2018	Moved switch to improve manufacturability
Rev E PCIe8LXMCX1	11/18/2018	Rolled revision to match PCB. Silk update
Rev 06	1/11/2019	Updated 5V and 3.3V power supplies to 15A model
Rev 07	4/21	Manufacturing update
Rev 08	7/23	Minor Silk-screen correction
Rev A PCIe4LXMCX1	1/12/2017	Release of PCIe4LXMCX1 board (4-lane version of the PCIe8LXMCX1 board)
Rev B PCIe4LXMCX1	4/27/2018	Updated to stay in sync with 8-lane model (PCIe8LXMCX1); various package size adjustments
Rev 03 PCIe4LXMCX1	3/25/2019	Updated 12V supply, 3.3V, and 5V to 15A

Manual Revision History

Table 2: Manual Revision History

Revision	Date	Description
A1	10/2/2012	Corresponds to Revision A/B of 10-2012-060(1,2)
A2	5/12/14	Corresponds to Revision A/B of 10-2012-060(1,2)
C1	10/30/2015	Corresponds to Revision C of 10-2012-0603 Added Jn6 pin assignment information Updated Warranty Policy Information
C2	8/24/2016	Corresponds to Revision C of 10/2012/0603 Updated name on cover page, 'Headers and Test Points', Warranty policy information, and 'Ordering Information'
C3	4/6/2017	Corresponds to Revision C of 10-2012-0603 (PCIe8LXMCX1) and 10-2017-0201 (PCIe4LXMCX1) Updated entire manual to reflect the addition of the PCIe4LXMCX1 version of the original PCIe8LXMCX1 board
04p1	6/26/2018	Corresponds to Revision C of 10-2012-060(3,4) (PCIe8LXMCX1) and 10-2017-020(1,2) (PCIe4LXMCX1) Updated to reflect changes made to hardware when revision was rolled
04p2	8/17/2020	Corresponds to Revision C of 10-2012-060(3,4) (PCIe8LXMCX1) and 10-2017-020(1,2) (PCIe4LXMCX1) Updated format to increase clarity and ease of use.
04p3	7/12/23	Add JTAG header definition, Revision 8 addition to Rev History

NOTE: Dynamic Engineering has made every effort to ensure that this manual is accurate and complete; that being said, the company reserves the right to make improvements or changes to the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

Product Description

PCIe8LXMCX1 and PCIe4LXMCX1 are referred to as PCIeNLXMCX1 in this manual. PCIeNLXMCX1 is part of the Dynamic Engineering PCIe- and XMC-Compatible family of modular I/O components. Both adapt an XMC to one PCIe slot. PCIeNLXMCX1 are ready to use with the default settings; simply install the XMC onto the board and then into the system.

Install PCIe8LXMCX1 into your PCIe system to adapt an XMC card. The XMC can have bezel and/or rear I/O. Pn4 and/or Pn6 are supported with PCIe8LXMCX1. 8 lanes are routed from the PCIe gold fingers to the XMC position. XMCs with up to 8 lanes can be used. The PCIe lanes to/from the XMC are routed per PCIe specifications with matched lengths and impedance control.

Install PCIe4LXMCX1 into your PCIe system to adapt an XMC card. The XMC can have a bezel and/or a rear I/O. Pn4 and/or Pn6 are supported with PCIe4LXMCX1. 4 lanes are routed from the PCIe gold fingers to the XMC position. Lanes 0-3 (4 total lanes) are connected, so you can fully support a 1-, 2-, or 4-lane XMC; cards with more than 4 lanes will likely work in a degraded mode, but it will depend on the XMC. Please refer to PCIe8LXMCX1 for up to 8 lanes of support, and contact Dynamic Engineering for 1- or 16-lane versions. The PCIe lanes to/from the XMC are routed per PCIe specifications with matched lengths and impedance control.

PCIeNLXMCX1 has two cooling cutouts for increased airflow to the XMCs. Fan positions are numbered 1-2. Position 1 is closest to the PCIe bezel (left edge in the picture on page ii). One fan can be mounted per position. Fans can be mounted to blow onto the XMC or pull air from the XMC. See the ‘Ordering Information’ section at the end of this document for more information regarding fan positions and other ordering options.

The individual pins on the Jn4 (Pn4) or Jn6 (Pn6) connectors for each slot are accessible by either a 68-pin SCSI connector or a 64-position DIN connector. The I/O are routed with matched-length, impedance-controlled differential traces suitable for single-ended and differential operation. Dynamic Engineering recommends using their SCSI cable and HDEterm68 breakout block with the SCSI connector. The industry standard VME IDC [DIN] connector is easy to connect to your system using DINterm64, which is a 64-position terminal strip, and the DIN Ribbon Cable 64, which is a 64-position cable.

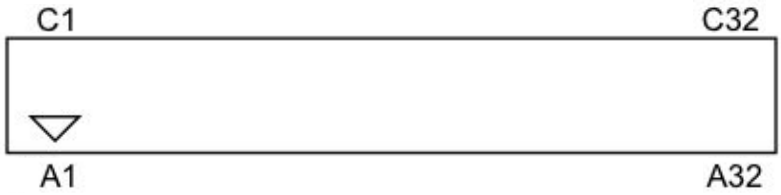
The XMC JTAG connections are routed to a header. Add “-JTAG” for this option; see the ordering information section of this manual for links to these.

The PCIe bus does not have a concept of global addressing. A DipSwitch is provided to allow the user to select the global address on the XMC position.

The PCIeNLXMCX2 has two options for Pn4 signal routing. VME style 2x32 pin header (shown on page ii) or SCSI style connector are available.

The “VME” connectors are oriented as shown in the photo on page ii of this manual and figure 1 below. The square pad in the photo is “A1”. The mating part number is 120-964-455 Panduit, DIN-IDCA-64CSB-TG30 Robinson Nugent. Berg also has a part that is slightly taller.

Figure 1: VME Connector Orientation



Cables and breakouts are available from Dynamic Engineering. Please see the ‘Ordering Information’ section of this manual for more information on DINterm64, DINribn64, HDEcabl68, and HDEterm68.

Key Product Features

Table 3: Key Product Features

Feature	Description
PCIe	Gen1, Gen2, Gen3
Voltage Monitors	On +12V, +5V, +12V, -12V Each has an LED that is illuminated when the voltages are within tolerance.
Regulators	15A regulator for XMC 3.3V and 5V supplies
Selection Switch for VPWR	12V or 5V Option for hardwired 5V or 12V
Connector access	Front panel connector access through the PCIe bracket
User I/O	Pn4 Available through one of two cable connectors (Din IDC or SCSI II compatible) Spare pins on SCSI connector can be shunt selected to 3.3V or ground
Thermal	Cooling cutout for increased airflow to XMCs component side Optional fan(s) with two mounting positions per XMC position
JTAG	XMC JTAG connections are tied to labeled header Programming support (-JTAG option)
DipSwitch	Supports global addressing on XMCs

Product Specifications

Table 4: Product Specifications

Specification	Description
Logic Interfaces	PCIe up to 8 lanes per XMC Gen1, Gen2, Gen3 compliant
Access Type	PCIe TLP transactions MSI interrupts
Clock rates supported	Gen1 – Gen 3
Software Interface	Passive design with no software required for adapter XMC register definitions as defined by installed hardware
Initialization	Switch selections for VPWR, bezel grounding, and cable options
I/O Interface	XMC bezel I/O supported at PCIe bracket Jn4/Jn6 “user I/O” supported with either SCSI or DIN connectors at both positions
Dimensions	½-length PCIe board
Construction	High-Temp FR4 Multi-Layer Printed Circuit, Through Hole, and Surface Mount Components.
Specification Compliance	XMC, PCIe specification compliant

Installation and Interfacing Guidelines

Some general interfacing guidelines are presented below. If you need more assistance, contact Dynamic Engineering.

Installation

Warning: Connection of incompatible hardware is likely to cause serious damage.

The XMC is mounted to PCIeNLXMCX1 prior to XMC installation within the chassis. For best results: with the PCIe bracket installed, install the XMC at an angle so that the XMC front panel bezel penetrates the PCI bracket, and then rotate it down to mate with the XMC connectors.

There are four mounting locations per XMC: two into the XMC mounting bezel and two for the standoffs near the XMC bus connectors.

Start-Up

Make sure that the “system” can see your hardware before trying to access it. Many BIOS will display the PCIe devices found at boot up on a “splash screen” with the VendorID and the CardID for the XMC installed and with an interrupt level. If the

information is not available from the BIOS, then a third-party PCIe device cataloging tool will be helpful. The device manager can be used for Microsoft Windows OS installations.

Guidelines

Grounds – Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should have all their own ground wires back to a common point.

Power Supply – Connecting external voltage to PCIeNLXMCX1 when not powered, can cause damage to the board and the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to installed XMCs than PCIeNLXMCX1 itself, and it is a smart system design when it can be achieved.

Thermal Considerations

PCIeNLXMCX1 features cooling cutouts designed to support the addition of a fan in one or two positions for each XMC. On PrXMCs and other XMCs with high thermal loads the fan option is recommended. The zero-slot fan option can provide plenty of cooling power should your XMC require it. On cards with a lower thermal profile, the fan is not needed. The fan produces 5 CFM in a small area to create a high LFM rating suitable for most cooling requirements.

DipSwitch Settings

Switch 1: Global Address settings

Position 1-3: correspond respectively to XMC GA0-2.
When closed, the signal is ‘0’. When open, the signal is ‘1’.

Position 4: corresponds to XMC-MVR0.
When closed, the signal is ‘0’. When open, the signal is ‘1’.

Positions 5-8 are spare

Construction and Reliability

PCIeNLXMCX1 is constructed out of 0.062-inch thick high-temp, RoHS compliant, FR4 material. Cooling cutouts have been designed into the product for improved air flow to the XMC sites. The components of PCIe4LXMCX1 and PCIe8LXMCX1 are tied into the internal power planes to spread the dissipated heat out over a larger area. This is an effective cooling technique in a situation where a large portion of the board has little or no power dissipation.

A fan option is available for high-thermal load XMCs or for chassis with a lack of air circulation.

Surface Mounted components are used. The connectors are SMT for the XMC bus and Through-Hole for the I/O.

The XMC Module connectors are keyed and shrouded with gold-plated pins on both the plugs and receptacles. They are rated at 1A per pin, 50 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The XMC Module is secured against the carrier with the XMC connectors. For enhanced security against vibration, the XMC mounting screws should be installed. The screws are supplied with the XMC from the OEM. Dynamic Engineering has screws, standoffs, blank bezels, and other XMC hardware available at a reasonable cost if your XMC was not shipped with some of the required attachment hardware or if it has been misplaced.

Power Supplies

The -12V, 5V and 3.3V for the XMC are regulated on board. The power supply designs utilize switching regulators to convert 12V. An LC filter ensures clean power at the XMC. The PCIe gold fingers are rated for 1.1A each and a total of 5.5A on the +12V rail. 55W are available to the XMCs after power conversion.

NOTE: this is the combined power requirement across the +12, -12, +5, and 3.3V power used by the XMCs. In most cases, 55W is sufficient.

PCIeNLXMCX1 has a cable connector to allow additional 12V power to be added to the card. The two supplies are diode coupled. In some cases, the 12V power supply on the backplane will not be adequately routed by the PC causing voltage to sag on the 12V. If this occurs, use the cable connector to compensate. (If 12V LED is off on cycling, this is an indication)

The power supplies include the bulk capacitance to properly bypass the FETs and post conversion voltage rails. Additionally, the XMC connectors are bypassed with a .1uF capacitor at each pin. The power supplies are checked with voltage monitor circuits. The LEDs are not illuminated unless the voltage is within the defined range.

A new feature on the revision 03 boards and later is the addition of selection headers to control the power sequencing of the 3.3V and 5V supplies. Some embedded systems reach the enumeration state very rapidly. When operating in a system with fast enumeration, the “no delay” mode should be selected. When operation is in “standard” setting and reducing the in-rush on the 12V supply, the “delay mode” selection is appropriate. When a power supply is not needed for your system, the power supply can be disabled to reduce in-rush requirements. For example, when the installed XMC does not use the 5V.

Three pin headers are supplied. When a shunt is installed in the “delayed” position, the corresponding power supply is enabled based on a local timer and the 12V supply reaching an operating level. In the “no delay” position, the power supply is enabled based on the 12V rail without the added delay. With no shunt installed, the power supply is disabled. The revision 1 and 2 boards were effectively operating in the delay

mode. Selection options exist to force the selection for users who do not want to be able to change the mode of operation.

The XMC specification calls out “VPWR”, which can be either 12V or 5V. PCIeNLXMCX1 has FET switching and a header to allow user selection of 12V, 5V, or neither voltage to be supplied to these 8 pins (per XMC). Build options are provided to allow “pre-selected” voltages on these pins without the headers. The 12V and 5V supplied are part of the same power budget mentioned above. It is suggested that the user select the rail definition most efficient for use, or alternatively, based on noise (the 5V will likely be quieter since it is converted on board and isolated from the 12V rail.

Pinout Options

J6 is used to select the VPWR source for position 0 and 1 respectively. When the shunt closes 1-2, 12V is selected. With 2-3 closed, 5V is selected. FETs are used to provide a low impedance path from the power supplies to VPWR. Options are in place on the PCB to allow hardwired selections for clients who prefer a fixed voltage. The headers are not installed when the fixed voltage option is in place. When pin 2 is open, VPWR will be open.

J12, 13 are used to select the bezel grounding option. 1-2 selects AC coupled, 2-3 selects DC coupled, and open is open. J13 = PCIe Bezel. J12 = XMC Bezel.

J1 is an optional header for SMB connection. Pin 1 is data and pin 2 is clock. Both are pulled up. Third party tools can be used to see the “innards” of the switch if the bus is in use. This is usually not needed, but it may be handy if you are doing development or want to walk or talk through the switch to the XMC positions.

TP1, TP2 are optional JTAG header/pwr used to connect to the XMC. 0.025” square post header. The pin definitions are in the silk. 1:3.3V, 2:GND, 3:TCK, 4:TDO, 5:TDI, 6:TMS, 7:TRST.

J2 controls the voltage on 33,67 of P2 when the SCSI connector options are selected. 1-2 selects 3.3V. 2-3 selects ground on those pins. The shunt and traces are rated for 1A. Not fuse protected.

J4, J5 control the power sequencing for 3.3V and 5V respectively. 1-2 selects a delayed start-up of the power supply. 2-3 for immediate start-up (based on 12V availability). Open is off (used for power savings when a supply is not required). Added with Revision 03 for the PCIe8LXMCX1 boards. Revision 01 for the PCIe4LXMCX1 boards. Resistor options are available to hardwire the selection.

XMC Module I/O Interface

The table below gives the pin assignments for the XMC Module I/O Interface from Jn4 to PCIe4LXMCX1 and PCIe8LXMCX1 connectors. See the User Manual for the XMC board being used for more information.

NOTE: P2 or P3, P4 or P5 are installed not both.

Table 5: XMC Module I/O Interface Pin Assignment

DIN IDC [P13]		SCSI II [P2]		Jn4		Jn6	
A1	C1	1	35	3	1	B1	A1
A2	C2	2	36	4	2	E1	D1
A3	C3	3	37	7	5	C2	C1
A4	C4	4	38	8	6	F2	F1
A5	C5	5	39	11	9	B3	A3
A6	C6	6	40	12	10	E3	D3
A7	C7	7	41	15	13	C4	C3
A8	C8	8	42	16	14	F4	F3
A9	C9	9	43	19	17	B5	A5
A10	C10	10	44	20	18	E5	D5
A11	C11	11	45	23	21	C6	C5
A12	C12	12	46	24	22	F6	F5
A13	C13	13	47	27	25	B7	A7
A14	C14	14	48	28	26	E7	D7
A15	C15	15	49	31	29	C8	C7
A16	C16	16	50	32	30	F8	F7
A17	C17	17	51	35	33	B9	A9
A18	C18	18	52	36	34	E9	D9
A19	C19	19	53	39	37	C10	C9
A20	C20	20	54	40	38	F10	F9
A21	C21	21	55	43	41	B11	A11
A22	C22	22	56	44	42	E11	D11
A23	C23	23	57	47	45	C12	C11
A24	C24	24	58	48	46	F12	F11
A25	C25	25	59	51	49	B13	A13
A26	C26	26	60	52	50	E13	D13
A27	C27	27	61	55	53	B15	A15
A28	C28	28	62	56	54	E15	D15
A29	C29	29	63	59	57	B17	A17
A30	C30	30	64	60	58	E17	D17
A31	C31	31	64	63	61	B19	A19
A32	C32	32	66	64	62	E19	D19
		33	67	Open, +3 or GND via J2,19 silk screen defined			
		34	68	Open, +3 or GND via J3,20			

Read table: [P13]:C1 = [P2]:35 = Jn4:1
[P13]:A1 = [P2]:1 = Jn4:3
Etc.

Warranty and Repair

Please refer to the warranty page on our website for the warranty and options that are currently offered.

www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify to the best of your ability, that the suspected unit is as fault. Then call the Dynamic Engineering Customer Service Department for a Return Material Authorization (RMA) number. Carefully package the product, in the original packaging if possible, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by anyone other than the original customer will be treated as out-of-warranty.

Out-of-Warranty Repairs

Out-of-warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the list price for one of that kind of unit. Return transportation and insurance will be billed as part of the repair in addition to the minimum RMA charge.

Contact:

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Ordering Information

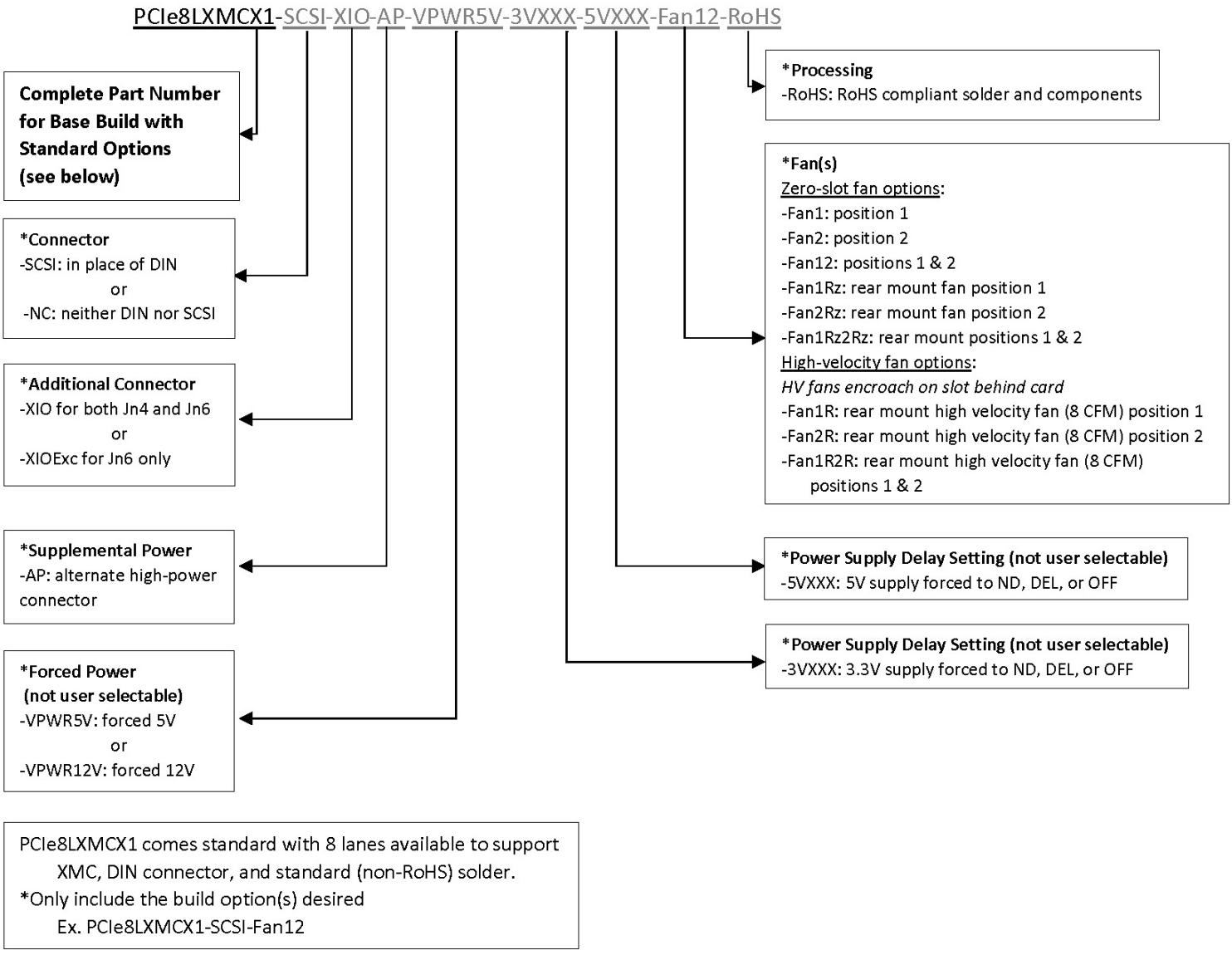
Standard Temperature Range-Rated Components: -40 - 85°C

Table 6: Ordering Information

Product	Description	
PCIe8LXMCX1	Comes standard with 8 lanes available to support XMC, DIN connector, and standard (non-RoHS) solder and components www.dyneng.com/PCIe8LXMCX1	
PCIe4LXMCX1	Comes standard with 4 lanes available to support XMC, DIN connector, and standard (non-RoHS) solder and components www.dyneng.com/PCIe4LXMCX1	
PCIe8LXMCX1 and PCIe4LXMCX1	**Options:**	
	-Fan_	Fan1 for position 1; Fan2 for position 2; Fan12 for both positions Low profile fans Push air toward the XMC
	-Fan_Rz	Fan1Rz; Fan2Rz; Fan1Rz2Rz Rear mount low-profile fans Pull air away from the XMC
	-Fan_R	Fan1R; Fan2R; Fan1R2R 8 CFM fan Only available as rear mount Pull air away from the XMC
	-SCSI	SCSI connector installed in place of the standard DIN connector
	-NC	No SCSI or DIN connector installed
	-RoHS	RoHS solder and components in place of standard
	-CC	Conformal coating
	-5VXXX	5V supply forced to (replace XXX). No Delay [ND], Delay [DEL], off [OFF] instead of user selectable
	-3VXXX	3V supply forced to (replace XXX). No Delay [ND], Delay [DEL], off [OFF] instead of user selectable
	-XIO	Comes with both Jn4 and Jn6 installed
	-XIOExc	Comes with only Jn6 installed (no Jn4)
	-VPWR5V	VPWR forced to 5V instead of user selectable
	-VPWR12V	VPWR forced to 12V instead of user selectable
	-AP	Alternate high-power connector installed for supplemental power. PC standard 2 row by 3 power cable receptacle Pins 1,2,3 = +12V Pins 4,5,6 = Ground (GND) **NOTE:** the standard card without the -AP option will work in most situations
HDEterm68	68-pin SCSI II to 68 screw terminal converter with DIN rail mounting www.dyneng.com/HDEterm68	

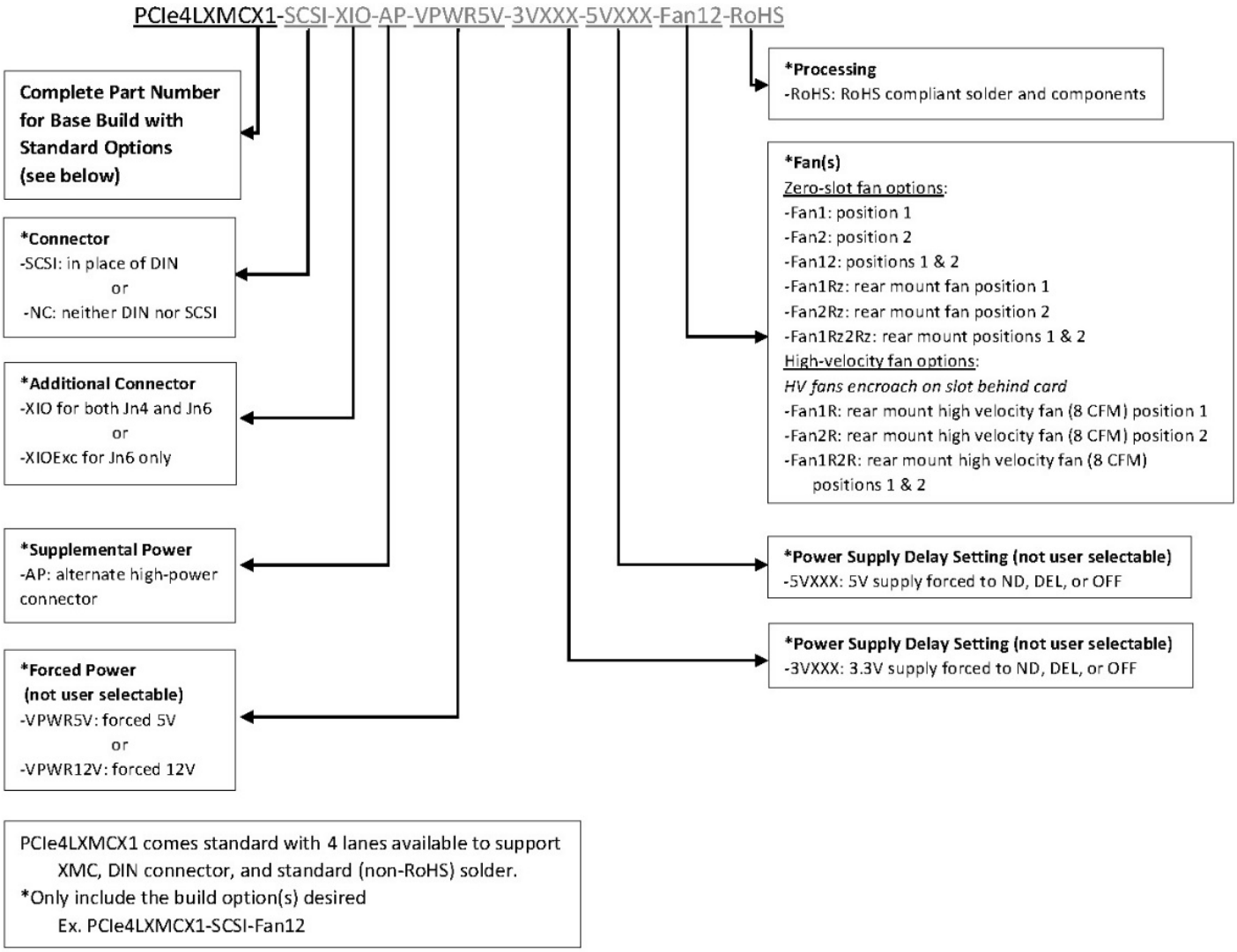
HDEcabl68	SCSI cables with latch blocks or thumbscrews. Various lengths available. Custom lengths can be ordered. www.dyneng.com/HDEcabl68
DINterm64	64-pin ribbon cable to 64 screw terminal converter with DIN rail mounting www.dyneng.com/DINterm64
DINribn64	64-pin ribbon cable with strain relief. Add -XX for number of inches. 36-inch is the default. www.dyneng.com/DINribn64

Figure 2: Ordering Options PCIe8LXMCX1



Dynamic Engineering PCIe8LXMCX1 Ordering Options Revision 01, July 31, 2020

Figure 3: Ordering Information PCIe4LXMCX1



Dynamic Engineering PCIe4LXMCX1 Ordering Options Revision 01, July 31, 2020

Glossary

Baud	Used as the bit period when talking about UARTs; Not strictly correct, but is the common usage when talking about UARTs.
CardID	Unique number assigned to a design to distinguish between all designs of a particular vendor
CFM	Cubic feet per minute
FIFO	First In First Out memory
Flash	Non-volatile memory used on Dynamic Engineering boards to store FPGA configurations or BIOS
JTAG	Joint Test Action Group – a standard used to control serial data transfer for test and programming operations.
LFM	Linear feet per minute
LVDS	Low Voltage Differential Signaling
MUX	Multiplexor – multiple signals multiplexed to one with a selection mechanism to control which path is active.
Packed	When UART characters are always sent/received in groups of four, allowing full use of host bus/FIFO bandwidth.
Packet	Group of characters transferred. When the characteristics of the group of characters is known, the data can be stored in packets and transferred as such; the system is optimized as a result. Any number of characters can be transferred.
PCI	Peripheral Component Interconnect – parallel bus from host to this device
PIM	PMC Interface Module (PIM). Provides rear I/O in cPCI systems. Mounts to PIM Carrier
PIM Carrier	PIM Mounting Device. Mounts on rear of cPCI backplane.
PMC	PCI Mezzanine Card – establishes common connectors, connections, size and other mechanical features.
TAP	Test Access Port – basically a multi-state port that can be controlled with JTAG [TMS, TDI, TDO, TCK]. The TAP States are the states in the State Machine that are controlled by the commands received over the JTAG link.
TCK	Test Clock provides synchronization for the TDI, TDO, and TMS signals

TDI	Test Data in – this serial line provides the data input to the device controlled by the TMS commands. For example, the data to program the FLASH comes on the TDI line while the commands to the state machine to move through the necessary states comes over TMS. Rising edge of TCK valid.
TDO	Test Data Out is the shifted data out. Valid on the falling edge of the TCK. Not all states output data.
TMS	Test Mode State – this serial line provides the state switching controls. '1' indicates to move to the next state, '0' means stay put in cases where delays can happen; otherwise, 0,2 are used to choose which branch to take. Due to the complexity of state manipulation, the instructions are usually precompiled. Rising edge of TCK valid.
UART	Universal Asynchronous Receiver Transmitter. Common serialized data transfer with start bit, stop bit, optional parity, optional 7/8 bit data. Can be over any electrical interface. RS232 and RS422 are most common.
Unpacked	When UART characters are sent on an unknown basis requiring single character storage and transfer over the host bus
VendorID	Manufacturers number for PCI/PCIe boards. DCBA is Dynamic Engineering's VendorID
XMC	Switched mezzanine card (PMC with PCIe)