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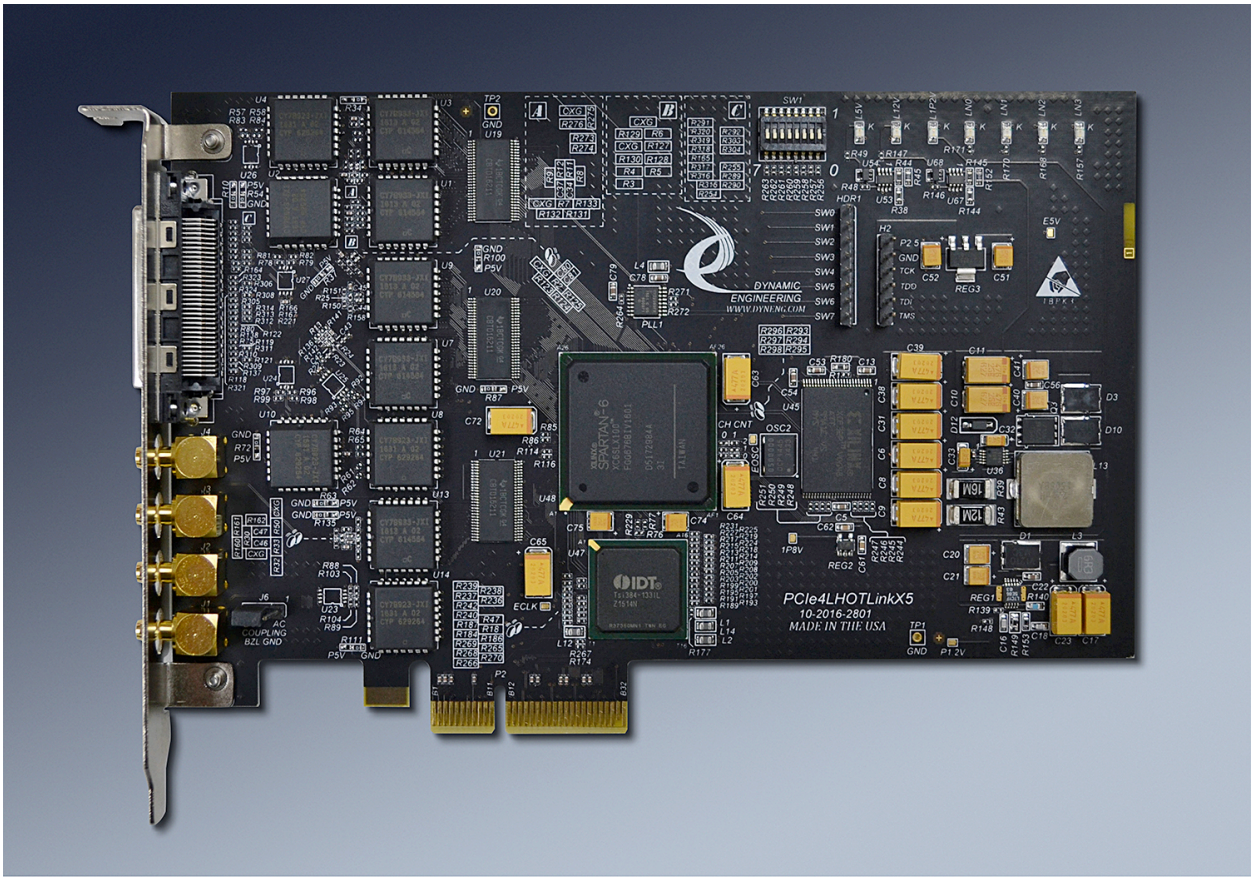
## User Manual

# PCIe4LHOTLinkX5-RV1

## Five-Channel HOTLink® Interface

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PCIe4LHOTLinkX5
PCIe Based Five-Channel
HOTLink® Interface

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## Product Description

The PCIe-HOTLink is part of the PCIe family of I/O components by Dynamic Engineering. It features the Cypress Semiconductor CY7B923/CY7B933 HOTLink® Transmitter/Receiver pair. The HOTLink devices use positive emitter-coupled logic (PECL) data inputs and outputs. See the block diagram below:

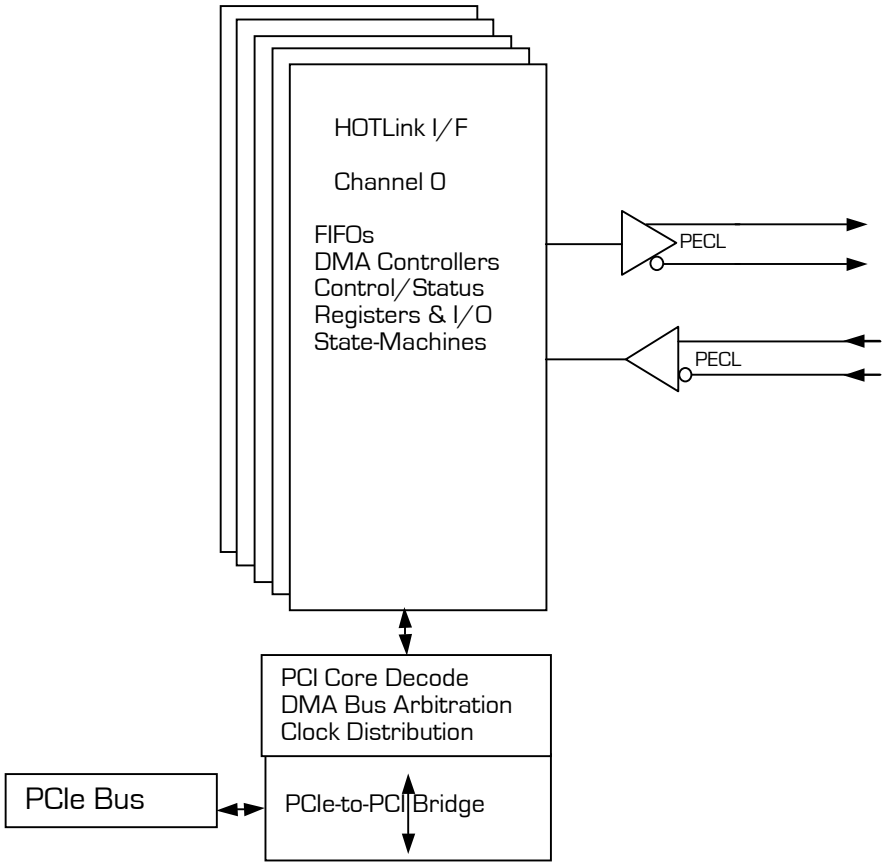



FIGURE 1 PCIE-HOTLINK BLOCK DIAGRAM

Up to five independent HOTLink channels are provided per card. Each HOTLink channel has two differential I/O signal pairs that can use either LVDS or PECL as a build option. When LVDS signaling is used, the input is connected across an equivalent 100 Ω shunt termination. The differential signals are then AC-coupled into the HOTLink receiver inputs referenced to 3.5 volts. The HOTLink differential output signals are biased to 3.3 volts and connected to a PECL-to-LVDS converter. When PECL signaling is used, each side of the differential input is terminated with 50 Ω to an equivalent 1.8 volts and then AC-coupled with 1000 pf to the HOTLink receiver referenced to 3.5 volts. The HOTLink differential output signals are biased to about 3 volts and AC-coupled with 1000 pf to the output connector. A single-ended on-board signal-path is also provided between each channel's HOTLink transmitter and receiver for built-in test capability.

The HOTLink receiver is supported by a 16k by 32-bit data FIFO; the HOTLink transmitter is supported by an 8k by 32-bit data FIFO. These FIFOs can be accessed by single-word read/writes as well as DMA burst transfers. The transmit FIFO supports write accesses only and the receive FIFO supports read accesses only, but a FIFO test bit in the channel control register enables the data to be routed from the transmit FIFO to the receive FIFO for a full 32-bit path for loop-back testing of the FIFOs.

The HOTLink board supports various interrupts. An interrupt can be configured to occur when the transmit FIFO is almost empty or the receive FIFO is almost full as well as other events and error conditions. All interrupt conditions can be individually masked and a channel master interrupt enable is provided to disable all interrupts on the channel simultaneously. The current real-time status is always available making it also possible to operate in polled mode.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please see our web page for current protocols offered and feel free to contact Dynamic Engineering with your custom application.

## Theory of Operation

The HOTLink board features a Xilinx Spartan-6-LX100 FPGA. The FPGA contains the PCI interface, all of the registers, FIFOs and protocol controlling elements for the HOTLink design. Only the PCI-to PCIe Bridge, HOTLink transceivers, I/O connectors, clock circuitry and power supplies are external to the Xilinx device.

A logic block within the Xilinx controls the PCI interface to the onboard PCI-to-PCIe Bridge. The HOTLink design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI core decode before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal. The PCI bus clock has been increased to 50 MHz to improve the data throughput of the board.

Scatter-gather bus-master DMA is provided for in this design. Once the physical address of the first chaining descriptor is written to the DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word that is the physical address of the first block of the IO buffer passed to the read or write call. The next four bytes represent a long-word indicating the length, in bytes, of that block. The final four bytes are a long-word that is the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is the direction bit and is set to one if the transfer is from the HOTLink board to host memory, and zero if the transfer is from memory to the board. All descriptor pointers, including the initial descriptor address written to start the DMA, must have the correct direction bit set. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one. This process continues automatically until the last chaining descriptor in the list is processed.

A PCIe-HOTLink channel has both a HOTLink receiver and transmitter. The transmitter is connected to the receiver input B by an always-on internal link from transmitter output C. Transmitter output A and Receiver input A are used for normal operation. Each channel’s input and output DMA engines interface with the channel’s HOTLink transmit and receive FIFOs respectively.

A control bit in the channel configuration register can be set to cause data written to the transmit FIFO to be immediately transferred to the receive FIFO where it can be read and verified to test the input and output FIFOs. The onboard HOTLink signal path can be enabled to test the HOTLink transceivers as well. Finally, I/O signals can be externally connected for a full loopback test of the entire circuit.

The PCIe-HOTLink-RV1 protocol used to transfer data from a transmitting node to a receiving node uses three control codes to indicate the start-of-header, end-of-header and end-of-data frame delimiters. The K28.1 control code indicates the start of the header portion of a data-frame. The K28.2 control code indicates the end of the header portion of a data-frame and the start of a data packet. The K28.3 control code indicates the end of a data packet. This can be followed by any number of additional data packets each terminated with a K28.3 control code or by a K28.1 start-of-header control code indicating the start of a new data-frame. In addition any number of idle or NULL control codes (K28.5) may be inserted in the character stream without affecting the resulting decoded data.

When these three control codes are stored to/from disc or other media, they are replaced by 64-bit quantities described as “Magic Words”. The start-of-header control code (K28.1) is replaced by the two 32-bit words 0x4FC5D059 followed by 0x01CB0135. The end-of-header control code (K28.2) is replaced by the two 32-bit words 0x4FC5D059 followed by 0x02CB0135. The end-of-data control code (K28.3) is replaced by the two 32-bit words 0x4FC5D059 followed by 0x03CB0135.

The transmitter reads 32-bit data-words from the transmit FIFO and when it detects one of the three defined magic word sequences, it replaces that eight-byte segment of data with the appropriate control code. When the receiver detects one of the defined control codes, it replaces it with the appropriate magic word sequence and writes the two 32-bit words to the receive FIFO.

# Programming

Programming the PCIe-HOTLink board requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI/PCIe subsystem. The base address refers to the first user address for the slot in which the board is installed. The VendorId = 0xDCBA. The CardId = 0x005F.

If DMA is to be used it will be necessary to acquire a block of non-paged memory that is accessible from the PCI bus in which to store chaining descriptor list entries. If the Dynamic Engineering device driver is used, the driver will handle all the DMA internal mechanics automatically.

Once the relevant enables and configuration options are set, the board will wait to receive HOTLink data and store it in a 16K by 32-bit FIFO. The FIFO almost full level is programmable to whatever level is desired and once that level is reached, an interrupt will be asserted if it has been enabled. The data can be read from the FIFO using DMA in an efficient manner.

The receive FIFO almost full and transmit FIFO almost empty levels are also used to control DMA channel preemption. When the receive or transmit preemption control bit is enabled, and the transmit FIFO is almost empty or the receive FIFO is almost full, other channels will be forced to relinquish the PCI bus so that the preempting channel can relieve the backlog.

The HOTLink receiver will continue to receive and store characters as long as it is enabled and there remains room in the receive FIFO.

# Address Map

| Register Name | Offset | Description |
|---|---|---|
| PHLRV1_BASE_CNTRL | 0x0000 | // Base Control register |
| PHLRV1_BASE_USER_INFO | 0x0004 | // Base User Info read port |
| PHLRV1_BASE_INT_STATUS | 0x0008 | // Base Interrupt Status read port |
| PHLRV1_CHAN_CNTRL_0 | 0x0020 | // Channel 0 Control register |
| PHLRV1_CHAN_STATUS_0 | 0x0024 | // Channel 0 Status register |
| PHLRV1_CHAN_FIFO_0 | 0x0028 | // Channel 0 TX/RX FIFOs single word access |
| PHLRV1_CHAN_WR_DMA_PNTR_0 | 0x002C | // Channel 0 Write DMA physical PCI dpr address |
| PHLRV1_CHAN_TX_FIFO_COUNT_0 | 0x002C | // Channel 0 Transmit FIFO data count |
| PHLRV1_CHAN_RD_DMA_PNTR_0 | 0x0030 | // Channel 0 Read DMA physical PCI dpr address |
| PHLRV1_CHAN_RX_FIFO_COUNT_0 | 0x0030 | // Channel 0 Receive FIFO data count |
| PHLRV1_CHAN_TX_AMT_0 | 0x0034 | // Channel 0 TX almost empty level |
| PHLRV1_CHAN_RX_AFL_0 | 0x0038 | // Channel 0 RX almost full level |
| PHLRV1_CHAN_SFP_0 | 0x003C | // Channel 0 SFP control/status |
| PHLRV1_CHAN_SFP_FIFO_0 | 0x0040 | // Channel 0 SFP FIFO port |
| PHLRV1_CHAN_TX_HDR_COUNT_0 | 0x0044 | // Channel 0 Byte count of last TX frame-header |
| PHLRV1_CHAN_TX_DATA_COUNT_0 | 0x0048 | // Channel 0 Byte count of last TX frame-data |
| PHLRV1_CHAN_RX_HDR_COUNT_0 | 0x004C | // Channel 0 Byte count of last RX frame-header |
| PHLRV1_CHAN_RX_DATA_COUNT_0 | 0x0050 | // Channel 0 Byte count of last RX frame-data |
| PHLRV1_CHAN_CNTRL_1 | 0x0054 | // Channel 1 Control register |
| PHLRV1_CHAN_STATUS_1 | 0x0058 | // Channel 1 Status register |
| PHLRV1_CHAN_FIFO_1 | 0x005C | // Channel 1 TX/RX FIFOs single word access |
| PHLRV1_CHAN_WR_DMA_PNTR_1 | 0x0060 | // Channel 1 Write DMA physical PCI dpr address |
| PHLRV1_CHAN_TX_FIFO_COUNT_1 | 0x0060 | // Channel 1 Transmit FIFO data count |
| PHLRV1_CHAN_RD_DMA_PNTR_1 | 0x0064 | // Channel 1 Read DMA physical PCI dpr address |
| PHLRV1_CHAN_RX_FIFO_COUNT_1 | 0x0064 | // Channel 1 Receive FIFO data count |
| PHLRV1_CHAN_TX_AMT_1 | 0x0068 | // Channel 1 TX almost empty level |
| PHLRV1_CHAN_RX_AFL_1 | 0x006C | // Channel 1 RX almost full level |
| PHLRV1_CHAN_SFP_1 | 0x0070 | // Channel 1 SFP control/status |
| PHLRV1_CHAN_SFP_FIFO_1 | 0x0074 | // Channel 1 SFP FIFO port |
| PHLRV1_CHAN_TX_HDR_COUNT_1 | 0x0078 | // Channel 1 Byte count of last TX frame-header |
| PHLRV1_CHAN_TX_DATA_COUNT_1 | 0x007C | // Channel 1 Byte count of last TX frame-data |
| PHLRV1_CHAN_RX_HDR_COUNT_1 | 0x0080 | // Channel 1 Byte count of last RX frame-header |
| PHLRV1_CHAN_RX_DATA_COUNT_1 | 0x0084 | // Channel 1 Byte count of last RX frame-data |

FIGURE 2 PCIE-HOTLINK REGISTER OFFSET ADDRESS MAP

| Register Name | Offset | Description |
|---|---|---|
| PHLRV1_CHAN_CNTRL_2 | 0x0088 | // Channel 2 Control register |
| PHLRV1_CHAN_STATUS_2 | 0x008C | // Channel 2 Status register |
| PHLRV1_CHAN_FIFO_2 | 0x0090 | // Channel 2 TX/RX FIFOs single word access |
| PHLRV1_CHAN_WR_DMA_PNTR_2 | 0x0094 | // Channel 2 Write DMA physical PCI dpr address |
| PHLRV1_CHAN_TX_FIFO_COUNT_2 | 0x0094 | // Channel 2 Transmit FIFO data count |
| PHLRV1_CHAN_RD_DMA_PNTR_2 | 0x0098 | // Channel 2 Read DMA physical PCI dpr address |
| PHLRV1_CHAN_RX_FIFO_COUNT_2 | 0x0098 | // Channel 2 Receive FIFO data count |
| PHLRV1_CHAN_TX_AMT_2 | 0x009C | // Channel 2 TX almost empty level |
| PHLRV1_CHAN_RX_AFL_2 | 0x00A0 | // Channel 2 RX almost full level |
| PHLRV1_CHAN_SFP_2 | 0x00A4 | // Channel 2 SFP control/status |
| PHLRV1_CHAN_SFP_FIFO_2 | 0x00A8 | // Channel 2 SFP FIFO port |
| PHLRV1_CHAN_TX_HDR_COUNT_2 | 0x00AC | // Channel 2 Byte count of last TX frame-header |
| PHLRV1_CHAN_TX_DATA_COUNT_2 | 0x00B0 | // Channel 2 Byte count of last TX frame-data |
| PHLRV1_CHAN_RX_HDR_COUNT_2 | 0x00B4 | // Channel 2 Byte count of last RX frame-header |
| PHLRV1_CHAN_RX_DATA_COUNT_2 | 0x00B8 | // Channel 2 Byte count of last RX frame-data |
| PHLRV1_CHAN_CNTRL_3 | 0x00BC | // Channel 3 Control register |
| PHLRV1_CHAN_STATUS_3 | 0x00C0 | // Channel 3 Status register |
| PHLRV1_CHAN_FIFO_3 | 0x00C4 | // Channel 3 TX/RX FIFOs single word access |
| PHLRV1_CHAN_WR_DMA_PNTR_3 | 0x00C8 | // Channel 3 Write DMA physical PCI dpr address |
| PHLRV1_CHAN_TX_FIFO_COUNT_3 | 0x00C8 | // Channel 3 Transmit FIFO data count |
| PHLRV1_CHAN_RD_DMA_PNTR_3 | 0x00CC | // Channel 3 Read DMA physical PCI dpr address |
| PHLRV1_CHAN_RX_FIFO_COUNT_3 | 0x00CC | // Channel 3 Receive FIFO data count |
| PHLRV1_CHAN_TX_AMT_3 | 0x00D0 | // Channel 3 TX almost empty level |
| PHLRV1_CHAN_RX_AFL_3 | 0x00D4 | // Channel 3 RX almost full level |
| PHLRV1_CHAN_SFP_3 | 0x00D8 | // Channel 3 SFP control/status |
| PHLRV1_CHAN_SFP_FIFO_3 | 0x00DC | // Channel 3 SFP FIFO port |
| PHLRV1_CHAN_TX_HDR_COUNT_3 | 0x00E0 | // Channel 3 Byte count of last TX frame-header |
| PHLRV1_CHAN_TX_DATA_COUNT_3 | 0x00E4 | // Channel 3 Byte count of last TX frame-data |
| PHLRV1_CHAN_RX_HDR_COUNT_3 | 0x00E8 | // Channel 3 Byte count of last RX frame-header |
| PHLRV1_CHAN_RX_DATA_COUNT_3 | 0x00EC | // Channel 3 Byte count of last RX frame-data |
| PHLRV1_CHAN_CNTRL_4 | 0x00F0 | // Channel 4 Control register |
| PHLRV1_CHAN_STATUS_4 | 0x00F4 | // Channel 4 Status register |
| PHLRV1_CHAN_FIFO_4 | 0x00F8 | // Channel 4 TX/RX FIFOs single word access |
| PHLRV1_CHAN_WR_DMA_PNTR_4 | 0x00FC | // Channel 4 Write DMA physical PCI dpr address |
| PHLRV1_CHAN_TX_FIFO_COUNT_4 | 0x00FC | // Channel 4 Transmit FIFO data count |
| PHLRV1_CHAN_RD_DMA_PNTR_4 | 0x0100 | // Channel 4 Read DMA physical PCI dpr address |
| PHLRV1_CHAN_RX_FIFO_COUNT_4 | 0x0100 | // Channel 4 Receive FIFO data count |
| PHLRV1_CHAN_TX_AMT_4 | 0x0104 | // Channel 4 TX almost empty level |
| PHLRV1_CHAN_RX_AFL_4 | 0x0108 | // Channel 4 RX almost full level |
| PHLRV1_CHAN_SFP_4 | 0x010C | // Channel 4 SFP control/status |
| PHLRV1_CHAN_SFP_FIFO_4 | 0x0110 | // Channel 4 SFP FIFO port |
| PHLRV1_CHAN_TX_HDR_COUNT_4 | 0x0114 | // Channel 4 Byte count of last TX frame-header |
| PHLRV1_CHAN_TX_DATA_COUNT_4 | 0x0118 | // Channel 4 Byte count of last TX frame-data |
| PHLRV1_CHAN_RX_HDR_COUNT_4 | 0x011C | // Channel 4 Byte count of last RX frame-header |
| PHLRV1_CHAN_RX_DATA_COUNT_4 | 0x0120 | // Channel 4 Byte count of last RX frame-data |

FIGURE 2(CONTINUED) PCIE-HOTLINK REGISTER OFFSET ADDRESS MAP

## Register Definitions

### PHLRV1_BASE_CNTRL

[0x000] Base Control (read/write)

| Base Control Register | |
|---|---|
| **Data Bit** | **Description** |
| 31-0 | Spare |

FIGURE 3 PCIE-HOTLINK BASE CONTROL REGISTER

There are no currently used control bits in the base control register.

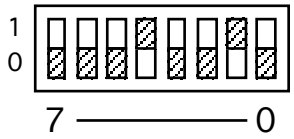
### PHLRV1_BASE_USER_INFO

[0x004] Base User Info – (read only)

| User Info Port | |
|---|---|
| **Data Bit** | **Description** |
| 31-24 | FPGA Design Revision |
| 23-16 | FPGA Design ID |
| 15-8 | PCI Core Revision |
| 7-0 | User ID Switch |

FIGURE 4 PCIE-HOTLINK BASE INFO PORT

User ID Switch: The user switch is read through this port. The bits are read as the lowest byte. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.




PCI Core Revision: This is the revision that was entered when the core was created, and is the value that is reported to the operating system. Currently this value is 0x00.

FPGA Design ID: This value distinguishes this design from other HOTLink designs using the same PCI vendor/device ID. For this design the value is 0x03.

FPGA Design Revision: The value of the fourth byte of this port is the revision number of the Xilinx design (currently 0x01 – rev A).

**PHLRV1_BASE_INT_STATUS**

[0x008] Base Interrupt Status – (read only)

**Base Interrupt Status Register**

| Data Bit | Description |
|---|---|
| 31-27 | Spare |
| 26-24 | Last Channel Implemented |
| 23-5 | Spare |
| 4-0 | Channel Interrupt Active |

FIGURE 5 PCIE-HOTLINK BASE STATUS PORT

Channel Interrupt Active: These five bits are used to report which channel's interrupts are active. When a one is read, it indicates that the corresponding channel has requested an interrupt; when a zero is read, that channel's interrupt is not active.

Last Channel Implemented: This three-bit binary field encodes the number of the last channel that is implemented on the board. From one to five channels can be populated and enabled on the PCIe-HOTLink-RV1 board. The number of the last channel must be between zero and four.

**PHLRV1_CHAN_CNTRL_0-4**

[0x020, 0x054, 0x088, 0x0BC, 0x0F0] Channel Control (read/write)

**Channel Control Register**

| Data Bit | Description |
|---|---|
| 31-29 | Spare |
| 28 | Receive Data Big-Endian Enable |
| 27 | Transmit Data Big-Endian Enable |
| 26 | Receiver Done Interrupt Enable |
| 25 | Transmitter Done Interrupt Enable |
| 24 | Transmitter Send Frame |
| 23 | Send Frame Auto-Clear Enable |
| 22-20 | Spare |
| 19 | Receiver BIT Enable |
| 18 | Receiver A Input Select |
| 17 | Transmitter Load Enable |
| 16 | Transmitter Output Enable |
| 15 | Transmitter BIT Enable |
| 14 | Receiver Enable |
| 13 | Transmitter Enable |
| 12 | Spare |
| 11 | Read DMA Arbitration Priority Enable |
| 10 | Write DMA Arbitration Priority Enable |
| 9 | Read DMA Interrupt Enable |
| 8 | Write DMA Interrupt Enable |
| 7 | RX FIFO Overflow Interrupt Enable |
| 6 | RX FIFO Almost Full Interrupt Enable |
| 5 | TX FIFO Almost Empty Interrupt Enable |
| 4 | Force Interrupt |
| 3 | Master Interrupt Enable |
| 2 | FIFO Data Loop-Back Test Enable |
| 1 | Receive FIFO Reset |
| 0 | Transmit FIFO Reset |

FIGURE 6 PCIE-HOTLINK CHANNEL CONTROL REGISTER

All bits are active high and are reset on system power-up or reset. If an external control or status bit is active low, it is inverted from the value in this register.

Transmit / Receive FIFO Reset: When one or both of these bits are set to a one, the corresponding data FIFO and control and status circuitry will be reset. When these bits are zero, normal FIFO operation is enabled. FIFO resets are synchronous, referenced to the PCI clock.

FIFO Data Loop-Back Test Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without sending data through the HOTLink interface. When this bit is zero, normal FIFO operation is enabled.

Master Interrupt Enable: When this bit is set to a one all enabled interrupts for the channel (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one a system interrupt will occur provided the channel master interrupt enable is set. This is useful to test interrupt service routines.

TX FIFO Almost Empty Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the transmit FIFO level is equal or less than the value specified in the PHLRV1_CHAN_TX_AMT register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register.

RX FIFO Almost Full Interrupt Enable: When this bit is set to a one, an interrupt will be generated when the receive FIFO level is equal or greater to the value specified in the PHLRV1_CHAN_RX_AFL register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register.

RX FIFO Overflow Interrupt Enable: When this bit is set to a one, an interrupt will be generated when an attempt is made to write to a full receive FIFO, provided the channel master interrupt enable is asserted. When a zero is written to this bit, an interrupt will not be generated when an overflow condition occurs, but the latched status can still be read from the channel status register.

Write / Read DMA Interrupt Enable: These two bits, when set to one, enable the DMA arbiter to use the TX almost empty and/or RX almost full status to give priority to a channel that is approaching the limits of its FIFOs. The levels written to the TX almost empty and RX almost full registers are used to determine these status values. When these bits are zero normal round-robin arbitration is used to determine access to the PCI bus for DMA transfers.

Write/Read DMA Arbitration Priority Enable: These two bits, when set to one, enable the DMA arbiter to use the TX almost empty and/or RX almost full status to give priority to a channel that is approaching the limits of its FIFOs. The levels written to the TX almost empty and RX almost full registers are used to determine these conditions. When these bits are zero normal round-robin arbitration is used to determine access to the PCI bus for DMA transfers.

Transmitter Enable: This bit, when set to one, enables the HOTLink transmitter state-machine. The behavior of the transmitter depends on the state of the Test Mode bit described above, whether there is data in the FIFO and whether the Send Frame control bit is set. When this bit is zero, the transmitter state-machine is disabled.

Receiver Enable: This bit, when set to one, enables the HOTLink receiver state-machine. The receiver will start storing data when either the specified start sequence is detected, or immediately if the receiver start mode is set to a one. The format of the stored data depends on the receive storage mode field described below. When this bit is zero, the receiver state-machine is disabled.

Transmitter BIT Enable: This bit, when set to one, enables the HOTLink transmitter Built-In-Test mode. When this bit is zero, Built-In-Test mode is disabled.

Transmitter Output Enable: This bit, when set to one, enables the external output of the HOTLink transmitter. When this bit is zero, only the internal output, which is always on, is enabled.

Transmitter Load Enable: When the Built-In-Test mode is enabled, setting this bit to a one starts the test sequence. This bit is zero in normal operation.

Receiver A Input Select: This bit, when set to one, selects input A of the HOTLink receiver. This input is driven by the AC-coupled external input. When this bit is zero, input B is selected. This input is driven by the internal signal coming from the channel's HOTLink transmitter output C.

Receiver BIT Enable: This bit, when set to one, enables the HOTLink receiver Built-In-Test mode. When this bit is zero, Built-In-Test mode is disabled.

Send Frame Auto-Clear Enable: When this bit is set to a one, the Transmitter send frame control bit will be automatically cleared when the frame completes. When this bit is zero, the send frame bit must be explicitly cleared.

Transmitter Send Frame: When this bit is set to a one, the transmitter will begin to send data-frames if the FIFO contains data. When this bit is zero, no frames will be sent.

TX/RX Frame Done Interrupt Enable: When one of these bits is set to a one, an interrupt will be generated when a transmit/receive frame completes. When this bit is zero, an interrupt will not be generated when a frame completes, but the status can still be read from the channel status register.

TX/RX Data Big-Endian Enable: When one of these bits is set to a one, the bytes of the relevant FIFO words are reversed. When this bit is zero, normal byte ordering is used. This byte re-ordering only affects the transmitted and/or received data-paths and has no effect on control/status register data.

**PHLRV1_CHAN_STATUS_0-4**

[0x024, 0x058, 0x08C, 0x0C0, 0x0F4] Channel Status Read/Latch Clear Write

**Channel Status Register**

| Data Bit | Description |
|---|---|
| 31 | Channel Interrupt Active |
| 30 | User Interrupt Active |
| 29 | Receiver I/O FIFO Full |
| 28 | SFP Ready (Idle) |
| 27 | SFP Programming Done (Latched) |
| 26 | SFP Programming Error (Latched) |
| 25 | Receive Framing Error (Latched) |
| 24 | Transmit Framing Error (Latched) |
| 23 | Received Data-Framing Synched |
| 22 | Receiver Running |
| 21 | Receive Frame Done (Latched) |
| 20 | Transmit Frame Done (Latched) |
| 19 | Transmit Data Read (Latched) |
| 18 | Receive Data Ready (Latched) |
| 17 | Read DMA Ready (Idle) |
| 16 | Write DMA Ready (Idle) |
| 15 | Read DMA Error (Latched) |
| 14 | Write DMA Error (Latched) |
| 13 | Read DMA Complete (Latched) |
| 12 | Write DMA Complete (Latched) |
| 11 | Receive Symbol Error (Latched) |
| 10 | Receive FIFO Overflow (Latched) |
| 9 | Receive FIFO Almost Full (Latched) |
| 8 | Transmit FIFO Almost Empty (Latched) |
| 7 | Receive Data Valid |
| 6 | Receive FIFO Full |
| 5 | Receive FIFO Almost Full |
| 4 | Receive FIFO Empty |
| 3 | Transmit Data Valid |
| 2 | Transmit FIFO Full |
| 1 | Transmit FIFO Almost Empty |
| 0 | Transmit FIFO Empty |

FIGURE 7 PCIE-HOTLINK CHANNEL STATUS REGISTER

Transmit FIFO Empty: When a one is read, the transmit data FIFO contains no data; when a zero is read, there is at least one data-word in the FIFO.

Transmit FIFO Almost Empty: When a one is read, the number of data-words in the transmit data FIFO is less than or equal to the value written to the PHLRV1_CHAN_TX_AMT register; when a zero is read, the level is more than that value.

Transmit FIFO Full: When a one is read, the transmit data FIFO is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Transmit Data Valid: When a one is read, there is at least one valid transmit data word left. This bit can be set even if the transmit FIFO is empty, because there is a one-word pipeline after the FIFO output to feed the transmit I/O or FIFO bypass path. When this bit is a zero, it indicates that there is no more valid transmit data.

Receive FIFO Empty: When a one is read, the receive data FIFO contains no data; when a zero is read, there is at least one data-word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data-words in the receive data FIFO is greater or equal to the value written to the PHLRV1_CHAN_RX_AFL register; when a zero is read, the level is less than that value.

Receive FIFO Full: When a one is read, the receive data FIFO for the channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Receive Data Valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO status reports empty, because there is a four-word pipeline after the FIFO output to facilitate a PCI read DMA. When this bit is a zero, it indicates that there is no more valid receive data.

Transmit FIFO Almost Empty (Latched): When a one is read, it indicates that the transmit FIFO data count has become less than or equal to the value in the PHLRV1_CHAN_TX_AMT register. A zero indicates that the FIFO has not become almost empty. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive FIFO Almost Full (Latched): When a one is read, it indicates that the receive FIFO data count has become greater than or equal to the value in the PHLRV1_CHAN_RX_AFL register. A zero indicates that the FIFO has not become almost full. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive FIFO Overflow (Latched): When a one is read, it indicates that an attempt has been made to write data to a full receive data FIFO. A zero indicates that no overflow condition has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Symbol Error (Latched): This is a latched version of the RVS (Received Violation Symbol) signal from the channel's HOTLink receiver. This bit is intended to be used for Built-In-Test operation as it indicates an error during the test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Write/Read DMA Complete (Latched): When a one is read, it indicates that the corresponding DMA transfer has completed. These bits are latched and must be cleared by writing the same bit back to this channel status port. A zero indicates that a corresponding DMA transfer has not completed since the bit was last cleared.

Write/Read DMA Error (Latched): When a one is read, it indicates that an error has occurred while the corresponding DMA was in progress. This could be a target or master abort or an incorrect direction bit in one of the DMA descriptors. These bits are latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no DMA error has occurred.

Write/Read DMA ready (Idle): These two bits report the DMA state-machine status. If a one is read, the corresponding DMA state-machine is idle and available to start a transfer. If a zero is read, the corresponding DMA state-machine is already processing a data transfer.

Receive Data Ready (Latched): This is a latched version of the ready signal from the channel's HOTLink receiver. This bit is intended to be used for Built-In-Test operation as the ready signal will pulse once per test loop, so polling this bit will indicate the completion of the receive test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Transmit Data Read (Latched): This is a latched version of the data read signal from the channel's HOTLink transmitter. Like the ready bit above, this bit is intended to be used for Built-In-Test operation as the data read signal will pulse once per test loop, so polling this bit will indicate the completion of the transmit test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Transmit Frame Done (Latched): When a one is read, it indicates that the transmitter has completed a data transfer. This is determined by the combination of all transmit data being sent and an end-of-data symbol being the last character sent. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that the transmitter has either not completed the transfer or no transfer was initiated.

Receive Frame Done (Latched): When a one is read, it indicates that the receiver has completed a data transfer. This is determined by the combination of idle characters at the receiver input following an end-of-data symbol. This bit is latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that the receiver has either not completed a transfer or a transfer was not initiated.

Receiver Running: When a one is read, it indicates that the receiver is actively processing I/O data. A zero indicates that the receiver is idle, either not enabled or waiting for a start-of-header character.

Received Data-Framing Synched: When a one is read, it indicates that the received data-stream is correctly framed, synchronized to the proper byte boundary. A zero indicates that the received data-stream is not frame-synched to a byte boundary.

Transmit Framing Error (Latched): When a one is read, it indicates that there has been a framing error in the transmit data stream. This indicates a control character that is out of sequence such as an end-of-data character before the start-of-data character or a start-of-header character within an already active frame. A zero indicates that there has not been a framing error since this bit was last cleared.

Receive Framing Error (Latched): When a one is read, it indicates that there has been a framing error in the received data stream. This indicates a control character that is out of sequence such as an end of data character before the start-of-data character or a start-of-header character within an already active frame. A zero indicates that there has not been a framing error since this bit was last cleared.

SFP Programming Error (Latched): When a one is read, it indicates that an error has occurred during an SFP write/read access. A zero indicates that there has not been an SFP programming error since this bit was last cleared.

SFP Programming Done (Latched): When a one is read, it indicates that an SFP access has completed successfully. A zero indicates that an SFP access has not completed successfully since this bit was last cleared.

SFP Ready (Idle): When a one is read, the SFP programmer is idle and ready to accept a new command; when a zero is read, the programmer is actively sending data or reading data to/from the SFP device.

Receiver I/O FIFO Full: When a one is read, it indicates that the 10-bit wide receiver input FIFO is full. A zero indicates that this FIFO is not full.

User Interrupt Active: When a one is read, it indicates that an enabled user interrupt condition (other than a DMA interrupt) is active. A zero indicates that no enabled user interrupt condition is active.

Channel Interrupt Active: When a one is read, it indicates that the interrupt is active for the referenced channel. A zero indicates that the channel interrupt is not active.

**PHLRV1_CHAN_FIFO_0-4**

[0x028, 0x05C, 0x090, 0x0C4, 0x0F8] TX FIFO Write/RX FIFO Read

| RX and TX FIFO Ports | |
|---|---|
| **Data Bit** | **Description** |
| 31-0 | FIFO data word |

FIGURE 8 PCIE-HOTLINK CHANNEL RX/TX FIFO PORT

These ports are used to make single-word accesses into the channel transmit FIFO and out of the channel receive FIFO instead of using DMA.

**PHLRV1_CHAN_WR_DMA_PNTR_0-4**

[0x02C, 0x060, 0x094, 0x0C8, 0x0FC] Input DMA Control (write only)

| Input DMA Pointer Address Port | |
|---|---|
| **Data Bit** | **Description** |
| 31-0 | First Chaining Descriptor Physical Address |

FIGURE 9 PCIE-HOTLINK CHANNEL WRITE DMA POINTER PORT

This write-only port is used to initiate a scatter-gather input DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit is set in one of the next pointer values. Writing a zero to this port will abort a write DMA in progress.

**PHLRV1_CHAN_TX_FIFO_COUNT_0-4**

[0x02C, 0x060, 0x094, 0x0C8, 0x0FC] TX FIFO Word Count (read only)

| TX FIFO Data Count | |
|---|---|
| **Data Bit** | **Description** |
| 31-14 | Spare |
| 13-0 | TX data words stored |

FIGURE 10 PCIE-HOTLINK CHANNEL TX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding transmit FIFO. The FIFO is 8,192 words deep and there is a 15-word auxiliary FIFO and three additional latches in the transmit data path that may contain data, which allows this value to be a maximum of 8,210 (0x2012).

**PHLRV1_CHAN_RD_DMA_PNTR_0-4**

[0x030, 0x064, 0x098, 0x0CC, 0x100] Output DMA Control (write only)

| Output DMA Pointer Address Port | |
|---|---|
| **Data Bit** | **Description** |
| 31-0 | First Chaining Descriptor Physical Address |

FIGURE 11 PCIE-HOTLINK CHANNEL READ DMA POINTER PORT

This write-only port is used to initiate a scatter-gather output DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive-e long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit is set in one of the next pointer values. Writing a zero to this port will abort a read DMA in progress.

**PHLRV1_CHAN_RX_FIFO_COUNT_0-4**

[0x030, 0x064, 0x098, 0x0CC, 0x100] RX FIFO Word Count (read only)

**RX FIFO Data Count**

| Data Bit | Description |
|---|---|
| 31-15 | Spare |
| 14-0 | RX data words stored |

FIGURE 12 PCIE-HOTLINK CHANNEL RX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding receive FIFO. The FIFO is 16,383 words deep and there are four additional latches in the read DMA pipeline that may contain data, which allows this value to be a maximum of 16,387 (0x4003).

**PHLRV1_CHAN_TX_AMT_0-4**

[0x034, 0x068, 0x09C, 0x0D0, 0x104] TX FIFO Almost Empty Level (read/write)

**TX FIFO Almost Empty Level Register**

| Data Bit | Description |
|---|---|
| 31-14 | Spare |
| 13-0 | TX FIFO almost empty level |

FIGURE 13 PCIE-HOTLINK CHANNEL TX FIFO AMT LEVEL

These read/write ports access the transmitter almost-empty level registers for the channel. When the number of data words in the transmit data FIFO is equal or less than this value, the almost empty status bit is set and an interrupt may be generated if it is enabled.

**PHLRV1_CHAN_RX_AFL_0-4**

[0x038, 0x06C, 0x0A0, 0x0D4, 0x108] RX FIFO Almost Full Level (read/write)

**RX FIFO Almost Full Level Register**

| Data Bit | Description |
|---|---|
| 31-15 | Spare |
| 14-0 | RX FIFO almost full level |

FIGURE 14 PCIE-HOTLINK CHANNEL RX AFL LEVEL

These read/write ports access the receiver almost-full level registers for the channel. When the number of data words in the receive data FIFO is equal or greater than this value, the almost full status bit is set and an interrupt may be generated if it is enabled.

**PHLRV1_CHAN_SFP_CNTROL_0-4**

[0x03C, 0x070, 0x0A4, 0x0D8, 0x10C] SFP Control/Status (write only)

**SFP Control Register**

| Data Bit | Description |
|---|---|
| 31-22 | Spare |
| 21 | Clear RVS Counter |
| 20 | SFP Test Enable |
| 19-12 | Byte Count |
| 11-4 | Start Address |
| 3 | SFP Diagnostic Enable |
| 2 | SFP Read Enable |
| 1 | Reset SFP Programmer |
| 0 | SFP Programmer Enable |

FIGURE 15 PCIE-HOTLINK CHANNEL SFP CONTROL

All bits are active high and are reset on system power-up or reset.

SFP Programmer Enable: When this bit is set to a one, the SFP programmer module, used to program and read the SFP, is enabled. When this bit is zero, the SFP programmer is disabled.

Reset SFP Programmer: When this bit is set to a one, the SFP programmer will stop processing, if not stopped already, and return to its initial state. When this bit is zero, the SFP programmer is ready to accept control inputs.

SFP Read Enable: When this bit is set to a one and the SFP programmer is enabled, the programmer will perform a read of the SFP device internal registers. When this bit is zero and the SFP programmer is enabled, the programmer will write data into the SFP device.

SFP Diagnostic Enable: When this bit is set to a one and the SFP programmer is enabled, the programmer will access the diagnostic address space (ID = 0xA2) instead of the normal address space (ID = 0xA0).

Start Address: This field specifies the register byte offset in the selected address space.

Byte Count: This field specifies the number of bytes to read/write. Beginning at the start address the internal registers of the SFP will be sequentially read or written.

SFP Test Enable: When this bit is set to a one, the SFP test function is enabled. When enabled, a 10 MHz clock is driven onto the SClk output pin. The RV1 test fixture allows this output pin to be connected to any of four input pins: Rx Signal Lost, Tx Fault, Module Not Installed or SDataIn. When the clock is detected on one of these status inputs, the continuity of that signal is confirmed. When this bit is zero, the test function is disabled and the signals operate normally.

Clear RVS Counter: When a one is written to this bit, the RVS counter is cleared. This counter is incremented by a received violation symbol pulse from the HOTLink receiver.

**PHLRV1_CHAN_SFP_STATUS_0-4**

[0x03C, 0x070, 0x0A4, 0x0D8, 0x10C] SFP Control/Status (read only)

**SFP Status Register**

| Data Bit | Description |
|---|---|
| 31-8 | RVS Count |
| 7 | SFP Read FIFO Empty |
| 6 | SFP Read FIFO Full |
| 5 | SFP Write FIFO Empty |
| 4 | SFP Write FIFO Full |
| 3 | Mod-Def2 (SData) Signal State |
| 2 | Receiver Loss-of-Signal Detected |
| 1 | Transmitter Fault Detected |
| 0 | No SFP Installed |

FIGURE 16 PCIE-HOTLINK CHANNEL SFP STATUS

No SFP Installed: This status bit reports the state of the MOD-DEF0 SFP signal. This signal is pulled-up on the PCIe-HOTLink-RV1 board. If no SFP module is installed, this signal will remain high. When the SFP module is installed, the MOD-DEF0 SFP signal is grounded through the SFP module and a zero will be read.

Transmitter Fault Detected: When a one is read, a transmitter hardware fault is indicated, such as a laser fault of some kind. When this bit is a zero, it indicates that the transmitter is operating normally.

Receiver Loss-of-Signal Detected: When a one is read, it indicates that the power of the received optical signal is below a minimum acceptable level. When this bit is a zero, it indicates that the receiver is operating normally.

Mod-Def2 (SData) Signal State: This status bit reflects the state of the SData signal. The SData signal along with the SClk signal are used to communicate with the SFP. This status bit is used to test the integrity of the OEN_N control line to the SFP using the RV1 test fixture. The OEN_N signal is connected to the SData signal through the test fixture, allowing the OEN_N signal to be monitored by reading the SData status bit. The SFP module is external to the board and not available for acceptance testing. The integrity of the control and status signals must be verified indirectly.

SFP Write FIFO Full: When a one is read, the SFP write data FIFO for the channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

SFP Write FIFO Empty: When a one is read, the SFP write data FIFO contains no data; when a zero is read, there is at least one data-word in the FIFO.

SFP Read FIFO Full: When a one is read, the SFP read data FIFO for the channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

SFP Read FIFO Empty: When a one is read, the SFP read data FIFO contains no data; when a zero is read, there is at least one data-word in the FIFO.

RVS Count: This 24-bit count is incremented by a received violation symbol pulse from the HOTLink receiver. The count reports the number of symbol errors that have occurred since the counter was last cleared.

**PHLRV1_CHAN_SFP_FIFO_0-4**

[0x040, 0x074, 0x0A8, 0x0DC, 0x110] SFP FIFO (read/write)

**SFP Output/Input FIFO Ports**

| Data Bit | Description |
|---|---|
| 31-0 | FIFO data word |

FIGURE 17 PCIE-HOTLINK CHANNEL SFP READ/WRITE FIFO PORTS

These ports are used to access the channel's read and write SFP data FIFOs.

**PHLRV1_CHAN_TX_FRM_HDR_BYTE_COUNT_0-4**

[0x044, 0x078, 0x0AC, 0x0E0, 0x114] Frame Byte-Count (read/write)

**Transmit Frame Header Byte Count Register**

| Data Bit | Description |
|---|---|
| 31-24 | Spare |
| 23-0 | Transmit Frame Header Byte-Count |

FIGURE 18 PCIE-HOTLINK CHANNEL TX FRAME HEADER BYTE COUNT

This register reports the number of bytes in the header section of the most recently transmitted data-frame.

**PHLRV1_CHAN_TX_FRM_DATA_BYTE_COUNT_0-4**

[0x048, 0x07C, 0x0B0, 0x0E4, 0x118] Inter-Frame Byte-Count (read/write)

**Transmit Frame Data Byte Count Register**

| Data Bit | Description |
|---|---|
| 31-24 | Spare |
| 23-0 | Transmit Frame Data Byte-Count |

FIGURE 19 PCIE-HOTLINK CHANNEL TX FRAME DATA BYTE COUNT

This register reports the number of bytes in the data section of the most recently transmitted data-frame.

**PHLRV1_CHAN_RX_FRM_HDR_BYTE_COUNT_0-4**

[0x04C, 0x080, 0x0B4, 0x0E8, 0x11C] Frame Byte-Count (read/write)

**Receive Frame Header Byte Count Register**

| Data Bit | Description |
|---|---|
| 31-24 | Spare |
| 23-0 | Receive Frame Header Byte-Count |

FIGURE 20 PCIE-HOTLINK CHANNEL RX FRAME HEADER BYTE COUNT

This register reports the number of bytes in the header section of the most recently received data-frame.

**PHLRV1_CHAN_RX_FRM_DATA_BYTE_COUNT_0-4**

[0x050, 0x084, 0x0B8, 0x0EC, 0x120] Inter-Frame Byte-Count (read/write)

**Receive Frame Data Byte Count Register**

| Data Bit | Description |
|---|---|
| 31-24 | Spare |
| 23-0 | Receive Frame Data Byte-Count |

FIGURE 21 PCIE-HOTLINK CHANNEL RX FRAME DATA BYTE COUNT

This register reports the number of bytes in the data section of the most recently received data-frame.

# Test Fixtures

## SFP Connector Pinouts

| Pin Number | Signal Name | Function/Description |
|---|---|---|
| 1 | VeeT | Transmitter Ground |
| 2 | TX Fault | Transmitter Fault Indication |
| 3 | TX Disable | Transmitter Disable |
| 4 | MOD-DEF2 | Module Definition 2 – Two wire serial interface (Data) |
| 5 | MOD-DEF1 | Module Definition 1 – Two wire serial interface (Clock) |
| 6 | MOD-DEF0 | Module Definition 0 – Grounded in module |
| 7 | Rate Select | Not Connected |
| 8 | LOS | Loss of Signal |
| 9 | VeeR | Receiver Ground |
| 10 | VeeR | Receiver Ground |
| 11 | VeeR | Receiver Ground |
| 12 | RD- | Inverse Received Data Out |
| 13 | RD+ | Received Data Out |
| 14 | VeeR | Receiver Ground |
| 15 | VccR | Receiver Power – 3.3V +/- 5% |
| 16 | VccT | Transmitter Power – 3.3V +/- 5% |
| 17 | VeeT | Transmitter Ground |
| 18 | TD+ | Transmitter Data In |
| 19 | TD- | Inverse Transmitter Data In |
| 20 | VeeT | Transmitter Ground |

FIGURE 22 PCIE-HOTLINK CHANNEL SFP CONNECTOR WIRING

1. TX Fault is an open collector/drain output, which should be pulled up with a 4.7K – 10KΩ resistor on the host board. Pull up voltage between 2.0 V and VccT, R+0.3 V. When high, output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V. By default, TX_FAULT is set to trigger on hardware faults only.
2. TX Disable input is used to shut down the laser output per the state table below with an external 4.7 - 10 KΩ pull-up resistor.
   Low (0 - 0.8 V): Transmitter on
   Between (0.8 V and 2.0 V): Undefined
   High (2.0 - 3.465 V): Transmitter Disabled
   Open: Transmitter Disabled
3. MOD-DEF 0, 1, 2. These are the module definition pins. They should be pulled up with a 4.7 - 10 KΩ resistor on the host board to a supply less than VccT +0.3 V or VccR+0.3 V.
   MOD-DEF 0 is grounded by the module to indicate that the module is present
   MOD-DEF 1 is clock line of two wire serial interface for optional serial ID
   MOD-DEF 2 is data line of two wire serial interface for optional serial ID
4. LOS (Loss of Signal) is an open collector/drain output which should be pulled up externally with a 4.7K - 10 KΩ resistor on the host board to a supply < VccT,R+0.3 V. When high, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). Low indicates normal operation. In the low state, the output will be pulled to < 0.8 V.
5. RD-/+: These are the differential receiver outputs. They are ac coupled 100Ω differential lines which should be terminated with 100Ω differential at the user SERDES. The ac coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 500 and 2000 mV differential (250 - 1000 mV single ended) when properly terminated.
6. VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.135 - 3.465 V at the SFP connector pin. The maximum supply current is 250 mA and the associated inrush current will be no more than 30 mA above steady state after 500 nanoseconds.
7. TD-/+: These are the differential transmitter inputs. They are ac coupled differential lines with 100Ω differential termination inside the module. The ac coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 500 - 2400 mV (250 - 1200 mV single ended), though it is recommended that values between 500 and 1200 mV differential (250 - 600 mV single ended) be used for best EMI performance.

| SFP Pin Number | Name | Chan0 P1 Pin Number | Chan1 P1 Pin Number |
|---|---|---|---|
| 1 | VeeT | 4 | 42 |
| 2 | TX Fault | 40 | 50 |
| 3 | TX Disable | 38 | 48 |
| 4 | MOD-DEF2 | 3 | 13 |
| 5 | MOD-DEF1 | 37 | 47 |
| 6 | MOD-DEF0 | 41 | 51 |
| 7 | Rate Select | — | — |
| 8 | LOS | 39 | 49 |
| 9 | VeeR | 6 | 44 |
| 10 | VeeR | 6 | 44 |
| 11 | VeeR | 6 | 44 |
| 12 | RD- | 35 | 45 |
| 13 | RD+ | 1 | 11 |
| 14 | VeeR | 6 | 44 |
| 15 | VccR | 3.3V | 3.3V |
| 16 | VccT | 3.3V | 3.3V |
| 17 | VeeT | 4 | 42 |
| 18 | TD+ | 2 | 12 |
| 19 | TD- | 36 | 46 |
| 20 | VeeT | 4 | 42 |

FIGURE 23 PCIE-HOTLINK CHANNEL SFP TEST FIXTURE WIRING

The above table describes two separate connection busses as there are two SFP connectors on the test fixture, one for each channel. The two SFP connectors are mounted on the test fixture PCB so that they are close to the connections for TD+/- and RD+/- and are aligned to the metal housing that encloses them and the two SFP optical transceivers.

Once the connectors, and housing are secured, and the SFP optical transceivers plugged in, fiber-optic connections can be made between HOTLink channel 0 and 1. Several status lines are connected from the SFP to the HOTLink board which are monitored from a memory-mapped status register. A two-wire communication bus is also present to read from and write to the SFP device's internal registers.

**HOTLink I/O Test Fixture**

An HDEterm-68 board is used for this test-fixture. The following connections are made on TP-1 with shielded twisted pair.

| Pin Num | From Sig Name | To Sig Name | Pin Num |
|---|---|---|---|
| 2 | HSSOut0+ | HSSIn1+ | 11 |
| 36 | HSSOut0- | HSSIn1- | 45 |
| 12 | HSSOut1+ | HSSIn2+ | 22 |
| 46 | HSSOut1- | HSSIn2- | 56 |
| 23 | HSSOut2+ | HSSIn3+ | 33 |
| 57 | HSSOut2- | HSSIn3- | 67 |
| 34 | HSSOut3+ | HSSIn0+ | 1 |
| 68 | HSSOut3- | HSSIn0- | 35 |

FIGURE 24 PCIE-HOTLINK CHANNEL I/O TEST FIXTURE WIRING

Two coax cables with SMB connectors are installed from J1 to J3 and J2 to J4.

A 10-pin header is installed in TP-2 starting at pin 3 ending at pin 41.
A 10-pin header is installed in TP-2 starting at pin 13 ending at pin 51.
A 10-pin header is installed in TP-2 starting at pin 24 ending at pin 62.
An 8-pin header is installed in TP-2 starting at pin 29 ending at pin 66.
A 7-pin header is installed in TP-2 starting at pin 18 ending at pin 21.

All pins of each of the five headers are tied together on the underside of the test fixture.

To test a channel's SFP status signals, a shunt is installed between TP-1 and TP-2 at the following pins:
pin 37 for channel 0
pin 47 for channel 1
pin 58 for channel 2
pin 66 for channel 3
pin 52 for channel 4

A second shunt is installed momentarily at the following pins:
pins 3, 39, 40 and 41 for channel 0
pins 13, 49, 50 and 51 for channel 1
pins 24, 60, 61 and 62 for channel 2
pins 32, 29, 30 and 31 for channel 3
pins 18, 19, 20 and 21 for channel 4

When the SFP test function is enabled, a 10 MHz clock is output on the SClk signal. When the shunts are installed, that clock will be detected on the various SFP status signals verifying those signals' integrity.

Another part of the SFP signal verification checks the OEN_N signals.

To test this signal, shunts are installed between TP-1 and TP-2 at the following pins:
pin 3 and pin 38 for channel 0
pin 13 and pin 48 for channel 1
pin 24 and pin 59 for channel 2
pin 32 and pin 65 for channel 3
pin 18 and pin 54 for channel 4

When the transmit output enable (active low) is asserted for a particular channel, the corresponding SData signal will go low verifying the integrity of the OEN_N signals (TX Disable on the SFP connector).

**HOTLink I/O Board-to-Board VHDCI to VHDCI Test Cable**

| Board 0 | | | Board 1 |
|---|---|---|---|
| Pin Num | From Sig Name | To Sig Name | Pin Num |
| 1 | HSSIn0+ | HSSOut0+ | 2 |
| 35 | HSSIn0- | HSSOut0- | 36 |
| 2 | HSSOut0+ | HSSIn0+ | 1 |
| 36 | HSSOut0- | HSSIn0- | 35 |
| 11 | HSSIn1+ | HSSOut1+ | 12 |
| 45 | HSSIn1- | HSSOut1- | 46 |
| 12 | HSSOut1+ | HSSIn1+ | 11 |
| 46 | HSSOut1- | HSSIn1- | 45 |
| 22 | HSSIn2+ | HSSOut2+ | 23 |
| 56 | HSSIn2- | HSSOut2- | 57 |
| 23 | HSSOut2+ | HSSIn2+ | 22 |
| 57 | HSSOut2- | HSSIn2- | 56 |
| 33 | HSSIn3+ | HSSOut3+ | 34 |
| 67 | HSSIn3- | HSSOut3- | 68 |
| 34 | HSSOut3+ | HSSIn3+ | 33 |
| 68 | HSSOut3- | HSSIn3- | 67 |

FIGURE 25 PCIE-HOTLINK BOARD-TO-BOARD TEST CABLE WIRING

This cable is used for the board-to-board tests where one board transmits on multiple channels and the other board receives on those same channels. The connections are bidirectional so that each board is tested as a transmitter and a receiver.

## P1 User Interface Pin Assignment

The figure provides the pin assignments for the PCIe-HOTLink P1 VHDCI connector.

| | | | |
|---|---|---|---|
| HSSIN_0+ | HSSIN_0- | 1 | 35 |
| HSSOUT_0+ | HSSOUT_0- | 2 | 36 |
| SDAT_0 | SCLK_0 | 3 | 37 |
| GND | TX_DIS_0 | 4 | 38 |
| GND | RX_LOS_0 | 5 | 39 |
| GND | TX_FAULT_0 | 6 | 40 |
| GND | MOD_N_0 | 7 | 41 |
| GND | GND | 8 | 42 |
| GND | GND | 9 | 43 |
| GND | GND | 10 | 44 |
| HSSIN_1+ | HSSIN_1- | 11 | 45 |
| HSSOUT_1+ | HSSOUT_1- | 12 | 46 |
| SDAT_1 | SCLK_1 | 13 | 47 |
| GND | TX_DIS_1 | 14 | 48 |
| GND | RX_LOS_1 | 15 | 49 |
| GND | TX_FAULT_1 | 16 | 50 |
| GND | MOD_N_1 | 17 | 51 |
| SDAT_4 | SCLK_4 | 18 | 52 |
| RX_LOS_4 | GND | 19 | 53 |
| TX_FAULT_4 | TX_DIS_4 | 20 | 54 |
| MOD_N_4 | GND | 21 | 55 |
| HSSIN_2+ | HSSIN_2- | 22 | 56 |
| HSSOUT_2+ | HSSOUT_2- | 23 | 57 |
| SDAT_2 | SCLK_2 | 24 | 58 |
| GND | TX_DIS_2 | 25 | 59 |
| GND | RX_LOS_2 | 26 | 60 |
| GND | TX_FAULT_2 | 27 | 61 |
| GND | MOD_N_2 | 28 | 62 |
| RX_LOS_3 | GND | 29 | 63 |
| TX_FAULT_3 | GND | 30 | 64 |
| MOD_N_3 | TX_DIS_3 | 31 | 65 |
| SDAT_3 | SCLK_3 | 32 | 66 |
| HSSIN_3+ | HSSIN_3- | 33 | 67 |
| HSSOUT_3+ | HSSOUT_3- | 34 | 68 |

FIGURE 26 PCIE-HOTLINK P1 INTERFACE

# Applications Guide

## Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

**ESD**
Proper ESD handling procedures must be followed when handling the PCIe-HOTLink. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

**Start-up**
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

**Watch the system grounds**
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

**We provide the components. You provide the system**. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

## Construction and Reliability

PCIe Modules while commercial in nature can be conceived and engineered for rugged industrial environments. The PCIe-HOTLink is constructed out of 0.062-inch thick FR4 material.

Surface mount components are used. Most devices are high pin count compared to mass of the device. For high vibration environments inductors and other higher mass per joint components can be glued down.

Conformal Coating is an option. For condensing environments conformal coating is required.

ROHS processing is an option. Standard lead solder is used unless “-ROHS” is added to the part number.

### Thermal Considerations

The PCIe-HOTLink design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

# Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

## Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

### Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

## For Service Contact:

Customer Service Department
Dynamic Engineering
150 Dubois Street, Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

## Specifications

| | |
|---|---|
| Host Interface: | Four-lane PCIe |
| Serial Interfaces: | Five HOTLink inputs and HOTLink outputs<br>Five SFP control/status interfaces |
| TX Bit-rates generated: | 250 MHz for the HOTLink I/O |
| Software Interface: | Control Registers, FIFOs, and Status Ports |
| Initialization: | Hardware reset forces all registers to 0 except as noted |
| Access Modes: | LW boundary Space (see memory map) |
| Wait States: | One for all addresses |
| Interrupt: | Each channel has an interrupt for TX done, RX done, TX almost empty, RX almost full and RX FIFO overflow. Read and write DMA interrupts are also implemented for each channel. |
| DMA: | Independent input and output Bus-Master Scatter/Gather DMA Support implemented for each channel |
| Onboard Options: | All Options are Software Programmable |
| Interface Options: | Channel 0-3 HOTLink receive and transmit lines are available on P1. Channel 4 transmit +/- available on J1/J2, receive +/- available on J3/J4. |
| Dimensions: | Standard Single PCIe board. |
| Construction: | FR4 Multi-Layer Printed Circuit, Surface-Mount Components |
| Power: | Max. **TBD** mA @ 12V<br>Max. **TBD** mA @ 3.3V |

## Order Information

| | |
|---|---|
| PCIe-HOTLink | http://www.dyneng.com/pciehotlink.html<br>Standard version with one 16K x 32-bit FIFO, and one 8K x 32-bit FIFO per channel. |

Win7 support is available with example test applications and source code.