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Software User's Guide (Linux)

PCIeAlteraCycloneIV

Re-configurable Logic
with RS-485/LVDS and TTL IO

PcieAlteraCycloneIV
Reconfigurable Logic
with RS-485/LVDS and TTL I/O

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Product Description

The PCIeAlteraCycloneIV provides a user configurable Cyclone IV FPGA along with 40 RS-485 or 40 LVDS transceivers, 8 PLLs (24 clocks), FIFO support and full DMA capabilities.

For a detailed description of the hardware including register definitions, see HW User Manual, PcieAlteraCycloneIVHwRevA1.

Software Description

The v1.0.0 PCIeAlteraCycloneIV driver contained in this release has been validated on an i7 Ubuntu SMP server running version 3.8.0-33 x86_64 kernel (64 bit).

This driver serves as an example framework for a custom driver utilizing existing HW logic, and a base for supporting customer specific functionality implemented in the Altera Cyclone IV FPGA. Beyond the functionality described below, all FPGA registers are accessible via IOCTL's. Register operations include Read, Write, and Read/Modify/Write.

The idea is to use the pre-defined IOCTL's for user design features retained from the reference design, and to use the Register Operation IOCTL's for the client specific parts of the design. In this manner any user changes can be accommodated without needing a new driver.

In addition the pre-defined IOCTL's can be reallocated by changing the include file to match any memory map changes made by the user.

Multiple levels of support are available to help our clients successfully use the driver, reference SW and PCIeAlteraCycloneIV. Please refer to the support program description for more information.
www.dyneng.com/TechnicalSupportFromDE.pdf

The driver implements the standard Linux char device driver. It supports read, write, and custom ioctl file operations. The read/write operations support both blocking and non-blocking modes. This release supports simultaneous operation of all 8 serial ports as well the parallel port. Ports 0-7 are serial, port 8 is parallel.

Ports must be configured after opening. The serial ports can be configured for internal loopback, or external I/O. Two internal loopback modes are supported, inner loopback wraps data back to the same port at the Xilinx FPGA. Outer

loopback wraps data back to the same port at the Altera Cyclone FPGA. If the external loopback fixture is attached, data is routed to the adjacent port (e.g 0->1, 2->3, 4->5, 6->7). Internal loopback operates in full-duplex mode, external I/O is half-duplex, and the direction must be set via the port configuration ioctl.

Parallel port direction is also set via the configuration ioctl.

By default, serial port reads/writes are optimized. If less than 11 words are to be transferred, single word accesses to the Rx/Tx FIFOs are utilized to avoid unnecessary overhead for small transfers, otherwise DMAs are utilized.

Depending upon specific system requirements, and the mix of I/O frame sizes, the user may configure a port to always utilize single word or DMA access. For example, if the data mix is mainly small frames with many back-to-back accesses, a port could be configured to utilize only DMA if CPU utilization is of greater concern than data throughput.

Ioctls are provided for programming/configuring the PLLs and the Altera Cyclone FPGA. Sample PLL and Cyclone configuration files are included with this distribution. If a Cyclone configuration file is loaded, all ports must be closed and re-opened after configuration is successfully completed.

Installation

1) Copy de_PciAltCycIV.c and de_PciAltCycIV.h to your module build directory. Invoke the system “make”
2) Copy the startup script bnm to the directory containing de_PciAltCycIV.ko.
3) Invoke the script (./bnm), it will create the devices required by the driver and performs an insmod of the module. You may invoke this script from the systems rc.local file as well

Application Programming model

After a port is opened, it must be configured for the desired mode of operation via the DE_CONFIG_PT ioctl. See de_PciAltCycIV.h for details of the parameters for this ioctl. Both blocking and non-blocking modes of operation are supported. This behavior is set via the standard file flags upon open.

Sample application

Two sample applications (de_IoApp.c, de_IoctlApp.c) are provided to demonstrate configuration, ioctl invocation, and I/O in the supported modes.

1) Compile the sample application for your platform, the output executable for these examples are dyn_io and dyn_ioctl.
    a. Nominal compilation gcc
       gcc –Wall –o dyn_io de_IoApp.c
       gcc –Wall –o dyn_ioctl de_IoctlApp.c
       The apps should compile without warnings, it is assumed de_PciAltCycIV.h is resident in the same directory as the applications for these examples.

I/O application invocation is as follows:

./dyn_io e|i|o|p port|port_group frame_len

The first parameter specifies which I/O mode (external, inner, outer loopbacks, or parallel). The second parameter specifies port or port group to be exercised. For inner or outer loopback, port range is 0..7. For external I/O with loopback fixture attached, port group range is 0..3. The last parameter specifies the frame length in long words to be transferred, range 1..8192. If parallel mode is specified port number and frame length are ignored.

Rx data is compared to Tx data upon read completion for each iteration when operating in serial mode.

Ioctl application invocation is as follows:
./dyn_ioctl e|i|o|p

A menu will be displayed:
Enter p(ll program)|c(onfig Altera)|r(eg ops)|l(ed ops)|e(xit)

The sample jed file (PAC4_1.jed) and rbf file (PcieAlterCycloneIV.rbf) are included in this distribution. The sample app assumes both of these files are resident in the same directory as the executable.

The Ioctl application demonstrates pll programming, FPGA configuration, register R/W/RMW operations. The LED test sequences through all LEDs several times with a delay so user may visually verify proper operation.

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Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

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