DYNAMIC ENGINEERING

150 DuBois St. Suite B&C Santa Cruz CA 95060
831-457-8891 https://www.dyneng.com
sales@dyneng.com
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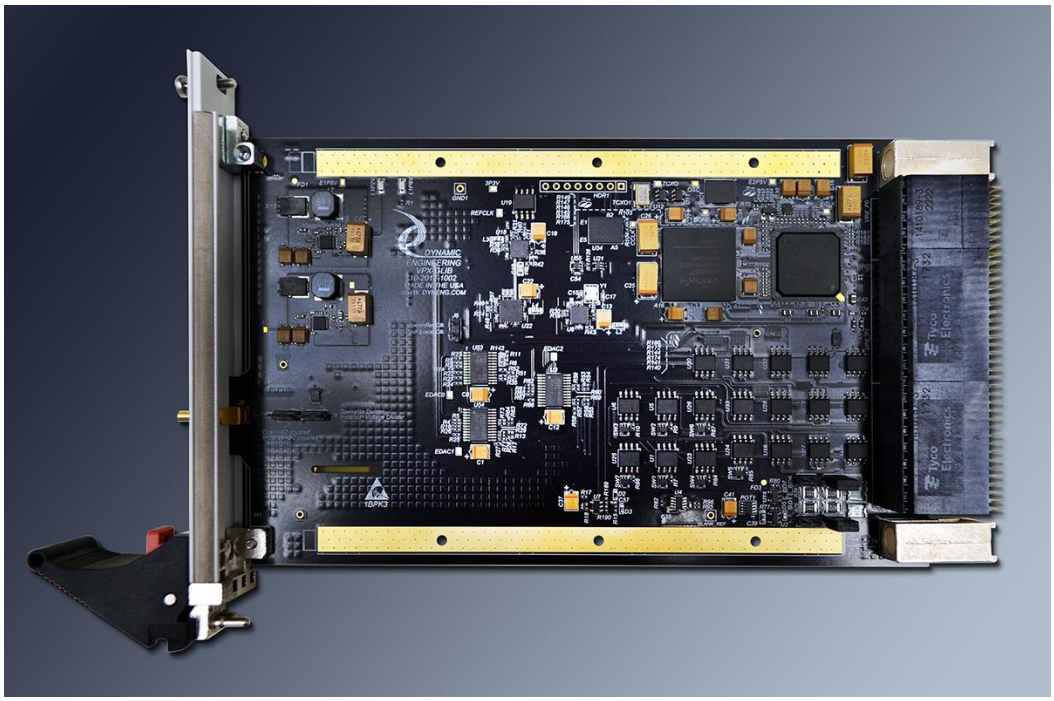
User Manual

VPX-GLIB

VPX 3U 4HP



Revision 02 shown without wedgelock option

Revision 2.0 11/25/24
Fab number 10-2017-1002

VPX-GLIB
3U 4HP

Dynamic Engineering
150 DuBois St Suite B&C
Santa Cruz, CA 95060
831-457-8891

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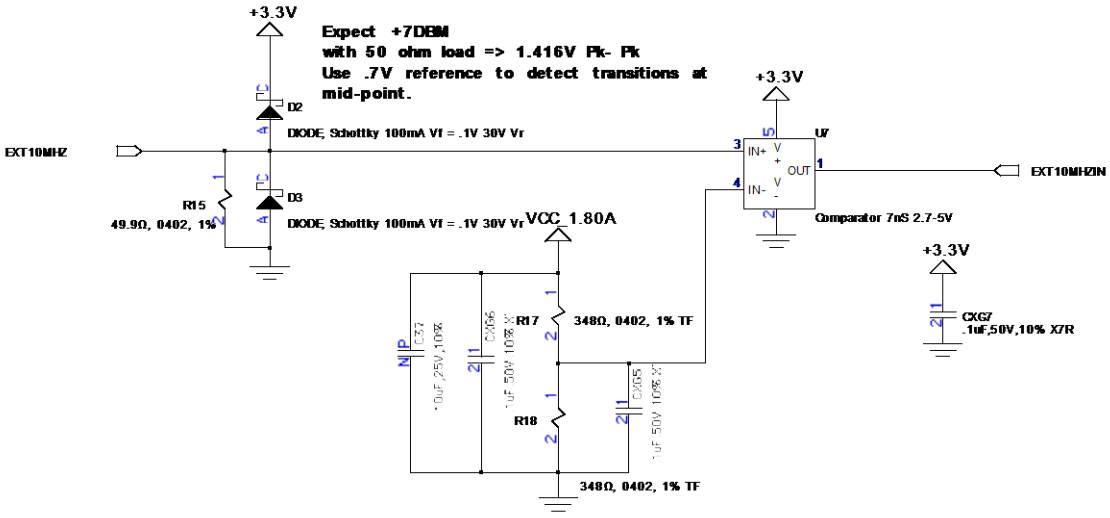
Product Description

VPX-GLIB is part of the Dynamic Engineering VPX compatible family of modular I/O components.

VPX-GLIB is a 3U 4HP design with optional wedge locks and built in cooling plane. Revision 2 of the PCB supports both SPI control [same as Rev 01] and PCIe control [new to rev 2].0

The bezel supplies a 10 MHz reference signal originating from a local TXCO or received 7 dbm reference signal. Both clocks are tested in the local FPGA against a 100 Mhz standard. SW can select which reference to output via the Coax connector.



All IO other than the above referenced coax are via the rear VPX IO connector [J2]. Control to the FPGA is provided with a SPI bus or PCIe access. The interface is implemented within a Spartan 6 FPGA. The control logic for the receiver and related interface hardware is also done within the FPGA.

Special features:

- VPX 3U 4HP
- SPI or PCIe access to Internal Registers
- SMB for Monitor function Voltage, temperature, fan speed
- 5V power from VPX used to generate 1.2, 1.8, 2.5
- 10 MHz clock reference LVTTL
- Misc Signal conversion to support CPU LVDS ⇔ RS485.
- Blanking Inputs with programmable thresholds, jumperable scaling resistors
- Remote Temperature sensor

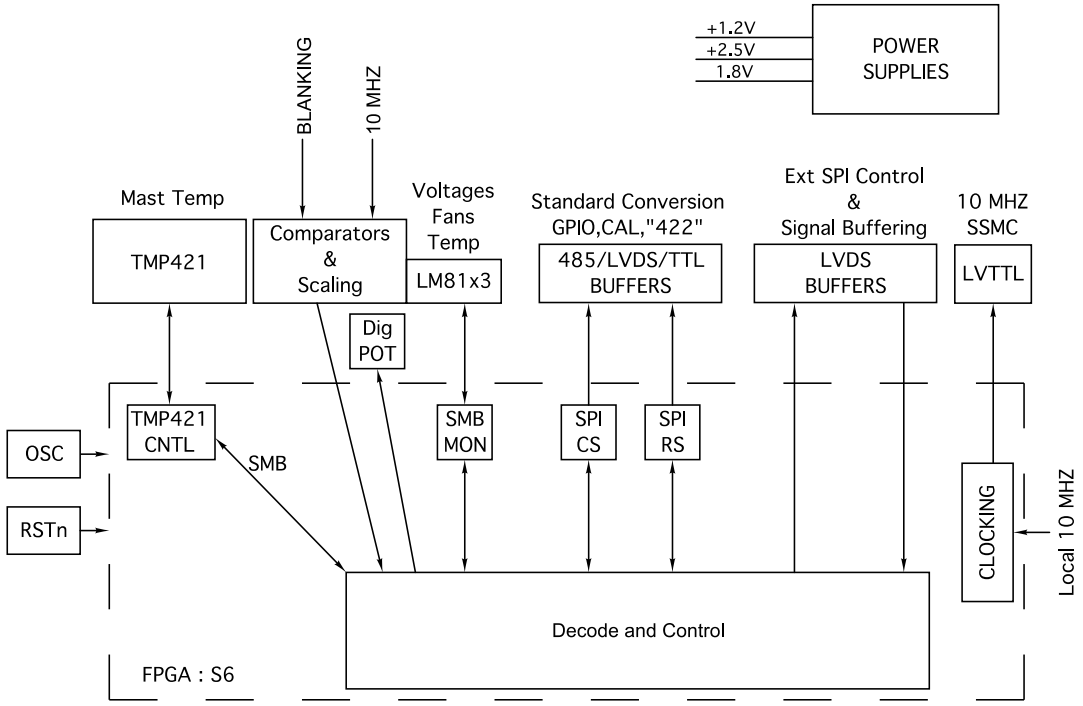


FIGURE 1 VPX GLIB BLOCK DIAGRAM

GLIB has many features and many details to cover. An outline of the features and basic capabilities is provided in this section of the manual. The detailed programming and use information is in the next section.

The diagram is simplified. Most of the interfaces shown have control and data registers. The register map is direct. The PCIe and SPI control buses operate in

parallel. You can set a register with one bus and read back on the other. The SMB interface is a little different in that the SMB control over the SPI interface is re-routed to the SMB devices based on the SPI address map. The PCIe access is via a new register allowing the same SW controlled interface to the SMB devices.

VPX-GLIB can be controlled via SPI. The SPI interface with the CPU is received and decoded. SPI accesses to internal functions are re-routed to a second decoder which extracts data to be written or packages data to be read. The extracted data is stored into a local register, and then parallel loaded to the target register. The size of the data is programmable within the VHDL. Messages of incorrect length are filtered – keeping the initial message and dumping the extra clocks. Each of the local registers has a separate data path [parallel] back to the encoder/decoder. The address received selects the mux output desired and the state-machine returns the requested data.

PCIe based accesses are decoded separately and tied to the SPI controlled path at the register. A common clock rate is used to operate allowing both paths to merge at the register. It is up to the user to prevent unexpected operation with both ports accessing the same register in parallel.

Functions that are external to the FPGA are routed there directly. The timing for those accesses are controlled by the CPU.

The FPGA receives 50 MHz from the oscillator. The clock input is doubled to 100 MHz and used locally for decoding SPI signaling and operating miscellaneous state-machines.

A TCXO oscillator provides a 10 MHz local reference. The local reference is compared with the external clock reference. Software can select the internal or external reference to be driven to the SSMC connector at the bezel. The selected clock is buffered with a 24 mA line driver.

The external 10 MHz is a +7dbm signal ⇔ 1.416 V pk-pk into 50 ohm load. The signal is diode protected to 3.3V and ground, terminated with 50 ohms, and compared with a .9V reference. The 1.8V reference is used along with local division and filtering to insure a quiet reference for this signal. The reference can be changed if necessary via the R17 & R18 resistor divider. Currently set to 348 ohms each to divide the 1.8 in half.

Two counters operate in parallel. One referenced to the the local 10 MHz and the other referenced to the external 10 MHz. The software can reset, start, and

set the end count for the internally referenced counters. For example the software can set a count corresponding to 1 mS of time counting. In addition, upper and lower limits are programmed. At the end of the test the value counted is checked against the limits and status is generated. Passing status is between the limits. The compared values and end counts are buffered and synchronized to allow changes to happen at any time. The value changes are implemented synchronously as well. The new values will be applied at the next opportunity for a check etc.

The clocks are buffered externally [to the FPGA] with a mux and line driver. The output from the line driver passes through a resister divider [2.2K in series and in parallel] and then through a .022uF capacitor. J8 [resistor] and J7 [cap] can be installed to selectively remove the Series components.

The FPGA converts the SPI bus to SMB format. Alternatively the internal SMB port can be used to create the SMB signals.

LM81 is a monitor circuit controlled with the SMB bus. The LM81 is initialized for operation, and then interrogated for Voltage levels, Fan speeds, and temperature. The device uses A/Ds to load the conversion values into memory. The LM81 stops updating when a value is read. It takes the better part of a second to update again. It is best to do a burst read of any values you are interesting in and then wait for the system requirement before doing it again. The LM81s can be programmed with upper and lower limits for each of the measurements and alarms generated if the values are out of bounds. Three LM81s are utilized to have enough voltage inputs for all of the signals to be monitored. Please see the programming section for details about which interface has which signals attached and what the scaling is for those inputs.

FLASH is used to reprogram the FPGA upon power up. The FPGA senses POR and initiates the reload of data. With Revision 2 the QSPI FLASH is programmed indirectly through the FPGA. The FPGA is connected via JTAG to the P0 VPX connector. To reprogram the P0 defined JTAG connector can be utilized along with Impact [Xilinx SW]. We used the PCIe8LSwVPX3U to interface to a PC and provide the JTAG connections.
https://www.dyneng.com/PCIe8LSwVPX3U.html

The VPX interface supplies 5V and 3.3V to VPX-GLIB. The 3.3V is used to run the supervisor circuit. When the 3.3V is within range the Reset signal is released to allow the FPGA to operate. Reset is connected in parallel with the PCIe reset to allow operation when the PCIe port is present or not in use.

EXT-GPIO is a bidirectional single ended LVTTL signal. The signal defaults to input and can be controlled via the SPI interface to be an output.

A second GPIO signal is provided with an LVDS buffer. Also programmable to operate as a receiver or transmitter with SW control.

TMP-422 is a remote junction temperature interface with an SMB connection. Internal and external temperatures are available. The control paths can be used to initiate initialization which loads some operating parameters from the internal FPGA registers to the TMP-422.

A second command causes a read of the device. The read polls the device to determine when a cycle has completed [Busy is(becomes) active busy becomes not active] and then read the local and external temperatures and stores those. Status is provided to allow the attached CPU to know when the new values are available. The device ID is returned at the end of initialization. TMP-422 responds with “22” when the ID is read.

The received single ended Blanking signals are first converted and then presented to the FPGA. The signals can be scaled with resistors coupled with shunts to reduce higher level signals. The signal path is FUSE – 4.7K – 1K – 1K pulldown - diode protection – comparator. The shunts allow the 4.7K and 1K series resistors to be eliminated. The comparator is referenced via a POT to allow SW to further scale when/how to respond to Blanking inputs. See headers and shunts section for specifics.

The POT is programmed by writing the POT value to a register. The references are set to 0 & 3.3V. There are 256 taps. The reference is therefore D/256 * 3.3V with a small offset. A testpoint is provided for the Blanking reference to allow checking of the programmed value. The ATP sets the POT to receive the Blanking inputs and provides a ramp for scope checking.

LVDS IO are provided for the output side of the blanking. These are hardwired to transmit. Three copies of Blanking 0 and one of Blanking 1 are provided.

Two sets of LVDS to 485, 485 to LVDS IO translation are provided. These IO default to the system standard and can be redefined in SW to reverse direction.

CAL MOD SW is expected to be an LVDS signal and is hardwired to be received.

The signal is routed to the FPGA.

The SPI interface is LVDS based and uses 7 transceivers to handle the DEV_EN, DEV_SEL(2-0), MOSI, MISO, CLK. The MISO signal is set to transmit with the rest set to receive.

Several of the transceivers are programmable for direction and in turn have programmable termination support. The terminations are set to 100 ohms with a 200 MHz rated analog switch to control the connection. Each switch is protected with a diode to prevent active differential pairs from “self powering” the GLIB.

Address Map

Name	SPI Address	Function
VpxGLIB _BASE_SPI_0	// VpxGLIB SPI Register offset 0 11 bits	misc functions
VpxGLIB _BASE_SPI_1	// VpxGLIB SPI Register offset 1 11 bits	LVDS/485 conversion
VpxGLIB _BASE_SPI_2	// VpxGLIB SPI Register offset 2 24 bits	check count lower
VpxGLIB _BASE_SPI_3	// VpxGLIB SPI Register offset 3 24 bits	check count upper
VpxGLIB _BASE_SPI_4	// VpxGLIB SPI Register offset 4 24 bits	clock check count
VpxGLIB _BASE_SPI_5	// VpxGLIB SPI Register offset 5 24 bits	TMP421 IF
VpxGLIB _BASE_SPI_6	// VpxGLIB SPI Register offset 6 12 bits	LM81 Tcrit, Int inputs,
VpxGLIB _BASE_SPI_7	// VpxGLIB SPI Register offset 7 8 bits	POT programming, TMP421 device ID input and status

The SPI control path is hardwired and local addresses used to select the device and functions within the device. SPI SEL is set to “000” to access these registers.

SPI SEL set to “010” to access external SMB devices [LM81].

Name	PCIe Address	Function
VpxGLIB _BASE_SPI_0	0x000000	misc functions
VpxGLIB _BASE_SPI_1	0x000004	LVDS/485 conversion
VpxGLIB _BASE_SPI_2	0x000008	check count lower
VpxGLIB _BASE_SPI_3	0x00000C	check count upper
VpxGLIB _BASE_SPI_4	0x000010	clock check count
VpxGLIB _BASE_SPI_5	0x000014	TMP421 IF
VpxGLIB _BASE_SPI_6	0x000018	LM81 Tcrit, Int inputs,
VpxGLIB _BASE_SPI_7	0x00001C	POT value, TMP421 device ID input and status
VpxGlib_TempRb	0x000020	Read-back of Reg5
VpxGlib_Rev	0x000024	Revision Register
VpxGlib_SmbCntl	0x000028	SMB control register
VpxGlib_SmbData	0x00002C	SMD Data read-back register

Vendor = xDCBA Device = x0076
PCIe addresses relative to Bar0 address.

Where the SPI register name is the same as the PCIe register name the register can be accessed from either port. Where unique to the PCIe address map the registers are only accessible from the PCIe side.

Bit Maps

VpxGLIB _SPI_0 Write

Bits	Function
10	ClockSelect
9	ICAL_DF_SW
8	ICAL_OM_SW
7	CntResetA
6-2	Spare
0	GPIO DIR

The size of the SPI port for read and write is “B”. The SPI address is Internal 0.

The Clock Select bit is used to select the internal TCXO source ‘0’ or the external received clock ‘1’. The clock selected is used to drive the coax signal via bezel connectors.

ICAL_DF_SW and ICAL_OM_SW determine the level driven on the respective signals. Both are hardwired to transmit within the FPGA. Both are fully connected to allow for direction control if required in the future.

CntResetA is combined with the POR to create a reset to the counters. When set to ‘1’ the counters are reset. Clear to ‘0’ for counting. See Clock count register.

GPIO DIR when set ‘1’ creates in on TTL and out on LVDS GPIO ports. When ‘0’ receive on LVDS and transmit on TTL. Signals are cross coupled with FPGA.

VpxGLIB _SPI_0 Read

Bits	Function
23-11	undefined
10	ClockSelect
9	ICAL_DF_SW
8	ICAL_OM_SW
7	CntResetA
6	‘0’
5	CntValid TCXO
4	CntValid Ext
3	INT BLNK2 IPS
2	INT BLNK1 IPS
1	GPIO DATA INS
0	GPIO DIR

10-7 and 0 bits are defined in the Write section.

The Count Valid status bits are the “real time” status for the clocks based on the programmed limits. If the count is within the range set, the status will be valid. Status is based on counting for the programmed length of time [number of counts]. The count status is updated based on the programmed length. The measurements are continuous.

INT BLNK bits provide the read capability of the input defined Blanking bits.

GPIO Data provides the current input GPIO level.

VpxGLIB_SPI_1

Bits	Function
23-11	undefined
10	Unused
9	Unused
8	Unused
7	DirLvdsPerIn
6	DirLvdsPerOut
5	Dir485PerIn
4	Dir485PerOut
3	TermLvdsPerIn
2	TermLvdsPerOut
1	Term485PerIn
0	Term485PerOut

The SPI port for this register matches the write port. The size of the SPI port for read and write is “B”. The SPI address is Internal 1.

Term bits when set ‘1’ asserts termination on that signal pair

Dir bits when set ‘1’ causes the direction on the transceivers to bit transmit.

LVDS and 485 are cross-connected in HW. All default to input. Set to one Rx and one Tx in the orientation desired. Normally the receiving side has the termination enabled.

Standard is LVDS PER IN = receive, 485 PER OUT = transmit and 485 PER IN = receive and LVDS PER OUT = transmit. See page 5 of schematic for more information.

VpxGLIB_SPI_2

Bits	Function
23-0	Clock Check Lower

VpxGLIB_SPI_3

Bits	Function
23-0	Clock Check Upper

VpxGLIB_SPI_4

Bits	Function
23-0	Clock Check Count

The SPI ports for these registers match the respective write ports. The size of the SPI ports for read and write is “x18”. The SPI addresses are Internal 2-4.

Count Check Lower is used to determine if the accumulated count is too low. Count Check Upper is used to determine if the accumulated count is too high. Clock Check Count is used to define the measurement period.

The 100 MHz. internal reference is used to count up to the programmed Clock Check Count. When the terminal count is reached the accumulated counts on the TCXO and External clock references are checked against the limits. If within the limits the status is set ‘1’. If not the status is cleared ‘0’. The Status remains in the determined state until the next measurement is completed. The status is meaningless until the limits and count period are established.

The limits are not included in the range [GT lower limit and LT upper limit is definition of “good” status].

Since the 100 MHz reference is faster than the 10 MHz expected rate be sure to use a large enough count to capture several counts on the 10 MHz.

The userap supplied with the driver has example code for programming these registers and checking the status,

VpxGLIB_SPI_5

Bits	Function	Write
23-16	TmpTC	Temp Correction
15-8	TmpCR	Conversion Rate
7-5	spare	
4	TmpRead	Set to Read
3-1	spare	
0	TmpInit	Set to Initialize

Bits	Function	Read
23-12	TmpLocal	PCB temperature at TMP device
11-0	TmpRemote	Remote temperature at PNP

The SPI read port for this register does not match the write port. The size of the SPI port for read and write is “x18”. The SPI address is Internal 5.

Write Definitions.

TmpTC is the definition to load to the n-factor Correction Register. We used the recommended 2N3906 transistor allowing the standard correction factor of 0x00 to be loaded here. Other transistor diode selections will need a value selected from the n-Factor Range Table in the TMP421-Q1 data sheet.

TmpCR is the definition of the Conversion Rate to use with the TMP device. See table 10 for the conversion rate vs programmed value. For power estimation the TMP device is referenced to 3.3V.

TmpInit is set to cause the hardware on the GLIB to initialize the TMP device by loading the TC and CR, starting conversions, and reading the device ID. When complete the bit is automatically cleared. The bit can be polled in register7 along with reading the ID.

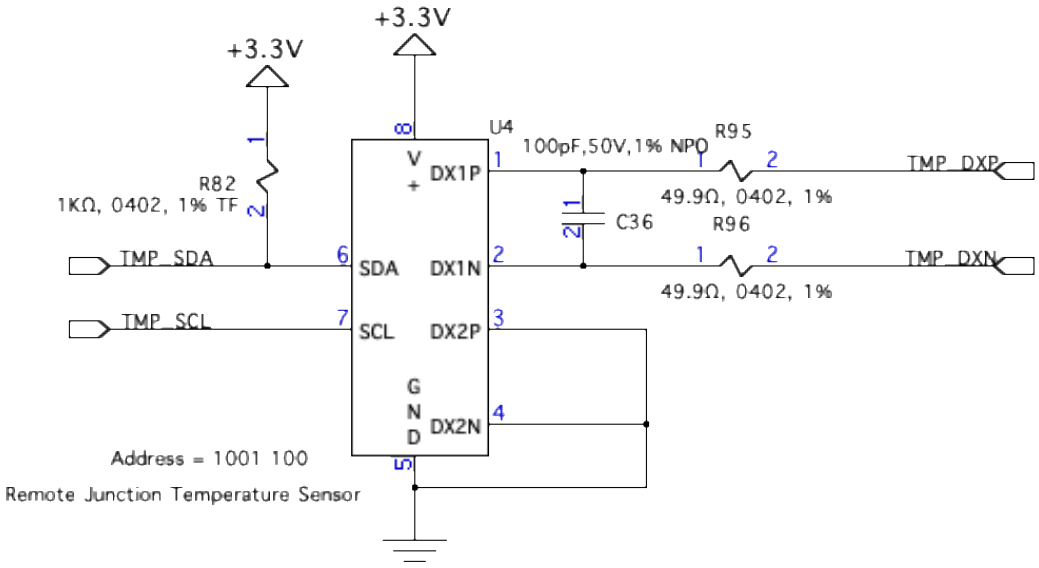
TmpRead is set to cause the hardware on the GLIB to read the TMP device. When complete the bit is automatically cleared. The bit can be polled in register7 along with reading the ID.

Read Definitions.

Reading from this port returns the last read internal and remote temperatures. The TmpRead function must be performed to receive meaningful data. The data is 16 bits with the upper 8 bits corresponding to the temperature in C above the decimal point. The lower 8 bits are encoded with the temperature below the decimal point. The lowest 4 bits are always zero and are not returned. ⇔ 11-4 = temperature in C [2's complement], 3-0 = value in C scaled with .0625. "0000" => .0, "0001" => .0625, "1111" => .9385. See tables 1 & 2 for more information.

Operation: The GLIB hardware takes care of most of the process.
1) Write the TC and CR definitions along with the Init bit set. Poll the INIT status [reg7] until cleared. Read the ID and validate = x22 for revision 2 boards.
2) Write with the Read bit set. TC and CR do not matter for this operation. Recommended to keep them set the way they were for the Init cycle for consistency. Poll Read status [reg7] until cleared. Read values and scale for your purposes. Note: HW will poll and wait for TMP422 to become busy [doing a conversion] and then wait until the conversion is completed. The amount of delay will depend on the CR setting.
3) Repeat number 2 as often as new temperature values are needed.

The recommended connection for TMP422 at the remote location is shown on the first page of the TMP421 family data sheet. TMP_DXP signal to emitter, TMP_DXN to base. Collector to local ground. For best performance the cabling should be low impedance and reasonably balanced between the two sides. Shielding may be necessary in electrically noisy environments.



Connection to TMP device. Revision 1 used the TMP-421. Revision 2 uses the TMP-422 as shown. The address is set based on the configuration as shown and matches the revision 1 implementation. The ID for the part responds with 22 for the Revision 2 and later boards.

VpxGLIB_SPI_6

Bits	Function
23-12	undefined
11	SMB TCRIT2NS
10	SMB TCRIT1NS
9	SMB TCRIT0NS
8	SMB INT2NS
7	SMB INT1NS
6	SMB INT0NS
5	SMB Reset
4	spare
3	spare
2	spare
1	spare
0	spare

The SPI read port for this register is different than the write port. The size of the SPI port for read and write is “C”. The SPI address is Internal 6.

SMB Reset is driven low with SMB Reset is ‘1’ otherwise tristated to allow the external pull-up to take the LM81s out of reset. Reset can be used to return the LM81s to a known state if your software has shutdown in the middle of an operation etc.

The SMB signals are the status bits from the LM81s for interrupt and temperature critical. The interrupt and temperature behavior is programmable within the LM81s. Please refer to the LM81 data sheet for those details. The “S” indicates the signals have be synchronized for reading.

Examples of interacting with the LM81 are contained in the UserAp software. The LM81 has many registers. The .H file may save some typing time as many of the registers are defined.

VpxGLIB_SPI_7

Bits	Function	Write
23-8	Undefined	
7-0	POT Data	

Bits	Function	READ
23-16	POT Data	
15-11	'0' for read	
10	PotBusy	
9	TmpRead	
8	TmpInit	
7-0	TmpID	

The size of the SPI port for read is "x18". Write is 8 bits. The SPI address is Internal 7.

Writing to the SPI interface will store the byte of data to program into the Digital Potentiometer and start the transmit state machine. The POT is programmed with 0-xFF corresponding to a range of 0V ⇔ ~3.3V.

The actual range is slightly above ground and slightly below the 3.3V rail. The Blanking Reference test point is provided to allow for easy measurements if you need to dial the offset in exactly. The testpoint is labled and on the edge of the PCB near the J2 connector.

The output from the Digital POT is used as a programming option for the Blanking comparators. Blanking is single ended and can be at varying input voltages. The combination of series resistors with shunts to short, a parallel termination, and the programmed reference voltage from the POT allow for a number of options. See the Headers and Shunts section for specifics.

Reading from the register returns the registered POT data [offset], plus the returned ID from the TMP422 and status for the TMP Initialization and Read commands, as well as the busy bit for the POT transfer.

TmpRead and TmpInit are set '1' when commanded to run those operations using SPI_5. When the process has completed the corresponding bit is cleared. These bits can be polled to see when initialization has completed and reading can begin.

TmpID returns the hardwired device ID from the TMP422 device. x22 is the expected value. If some other value is read, re-run the Initialization process. If

the value is still not x22 a hardware issue of some sort exists.

PotBusy is set ‘1’ during the time the current command is being transferred to the POT. The transfer occurs at 3.57 MHz and is only 8 clocks long. There is some additional overhead to synchronize between the SPI internal clock 50 MHz and the POT clock. Status should be ‘0’ “not Busy” when writing a new command to load the POT.

VpxGLIB_TempRb

Bits	Function	Write
23-16	TmpTC	Temp Correction
15-8	TmpCR	Conversion Rate
7-5	spare	
4	TmpRead	Set to Read
3-1	spare	
0	TmpInit	Set to Initialize

This PCIe port is offset x20 and provides read-back capability of register 5 – The TMP422 interface control. The bit definitions are repeated here for convenience. For the expanded information please refer to the Register 5 definition.

VpxGLIB_Rev

Bits	Function
15-8	Revision Major
7-0	Revision Minor

This PCIe port is offset x24 and provides read-back capability of the Flash revision. Currently 2.1 for the Major.Minor revision

VpxGLIB_SmbCntl

Bits	Function
31	Port Select
30-2	Spare
1	MOSI
0	Clk

VpxGLIB_SmbData

Bits	Function
31-1	Spare
0	MISO

This PCIe port is offset 0x28 for the Regs Register and x2C for the Data port.

The Cntl port is read/write with the current register value returned. The data input from the SMB device is in the Data port.

The Clk, MOSI, MISO, and Port select signals are added to the primary SPI decoder and when Port Select is set to '1' used to control the external SMB port. The Default for the Port Select is '0' [reset condition] providing the SPI bus control over the SMB port.

Use "bit banging" to create the SMB stream to access the 3 SMB devices. The UserAp has an example of this procedure and further examples of reading all of the voltages, temperature, and fan speed values. The test software expects a test fixture to be connected to provide the voltages and FAN signals.

VpxGLIB _SPI

VPX-GLIB is controlled via SPI and PCIe bus operations. To facilitate we used a PMC-BiSerial-VI with modifications to provide the opposite side of each of the P2/J2 referenced interfaces including the SPI interface. PCIeBPMCX1 is used to interface the PMC-BiSerial-VI to the computer, a SCSI cable from the BiSerial to the PCIe8LSwVPX3U provided the IO path, and the VPX was mounted to the PCIe based adapter. The PCIe path is from the host computer through the carrier [PCIe8LSwVPX3U]. We used the Ref Clk between the carrier and VPX to generate the local PCIe clock.

The register is used for “bit banging” to generate the SPI interface for test purposes.

MOSI [master out slave in] signal to write data to VPX-GLIB .

MISO is the return data path from VPX-GLIB and is tied to MISO through the loop-back described above and documented in the loop-back section.

DevSelx are used to set the 1st level address for the SPI bus. The first level is used by VPX-GLIB to interconnect the SPI bus with the correct hardware. Within the SPI message can be further address and data information to be decoded by the target device.

Address	Destination
0	Local
1	Local
2	SMB
3-7	Spare

The local addresses within the VPX-GLIB are decoded from the DevSel 0 or 1. The upper address range is not used at the moment. The first 8 registers are used from the lower range (0). The register bit definitions preceed this section.

The local SPI interface protocol is based on an initial byte of local address followed by the data to write or the data read back. There is a 1 clock delay for the read data. The lengths for each of the registers are shown in the various bit map descriptions. The hardware is set-up to allow quick changes for register size.

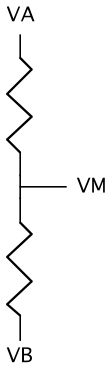
The SMB bus is half duplex while the SPI is full duplex. VPX-GLIB takes care of the expansion / multiplexing automatically. Remember to keep MOSI high when not transmitting and selecting the SMB bus.

The LM81s are on the SMB bus. The addresses are set to 0, 1 and 2 which corresponds to x58, x5A, x5C respectively [with R/W set to W]. The device connections are as follows: [see page 13 of the schematic for more information]

Function	Device 0	Device 1	Device 2
Fan1	FAN1TACH	FAN3TACH	Spare
Fan2	FAN2TACH	FAN4TACH	Spare
V12	Int 12V	12VA	12VC
V5	Int 5V	5VA	gnd
V3.3	Int 3.3V	12VB*	12VD*
V2.5	Int 2.5V	15VB*	15VC*
Vccp1	-8VA*	-15VA*	-15VB*
Vccp2	spare	15VA*	8VA*

* indicates voltage scaled to meet input definition
Lettered voltages are external levels – see P2/J2 definition

The LSB size is different for the different inputs for the LM81 based on the scaling in place within the device. 13mV for 2.5, 17.2mV for 3.3V, 26 mV for 5V, 62.5mV for 12V, and 14.1mV for the VCCp inputs.



Please see below for scaling definitions.

Device 0 : Vccp1 on is used to measure -8VA.
3.3V (VA) is tied through a 30.1K resistor (R1) to 135.2K (R2) to –8V (VB) with the node between (VM) the resistors going to the VCCp1 input.

It is suggested that the 3.3V measurement be taken first and then used when calculating the –8V value. The math is in the LM81 data sheet and a reference for programming in the userap software.

Device 1:
+12 is measured on the 3.3V input:
VA = 12, VB = GND, R1 = 76.8K, R2 = 29.4K.
+15 is measured on the 2.5V input:
VA = 15, VB = GND, R1 = 49.9K, R2 = 10K.

-15 is measured on the VCCp1 input:
VA = 3.3, VB = -15, R1 = 31.6K, R2 = 249K.

+15 is measured on the VCCp2 input:
VA = 15, VB = GND, R1 = 56K, R2 = 5.1K.

Device 2:
+12 is measured on the 3.3V input:
VA = 12, VB = GND, R1 = 76.8K, R2 = 29.4K.

+15 is measured on the 2.5V input:
VA = 15, VB = GND, R1 = 49.9K, R2 = 10K.

-15 is measured on the VCCp1 input:
VA = 3.3, VB = -15, R1 = 31.6K, R2 = 249K.

+8 is measured on the VCCp2 input:
VA = 8, VB = GND, R1 = 22K, R2 = 4.02K.

All resistors are 1%. Some are combinations where the parallel / series value is shown.

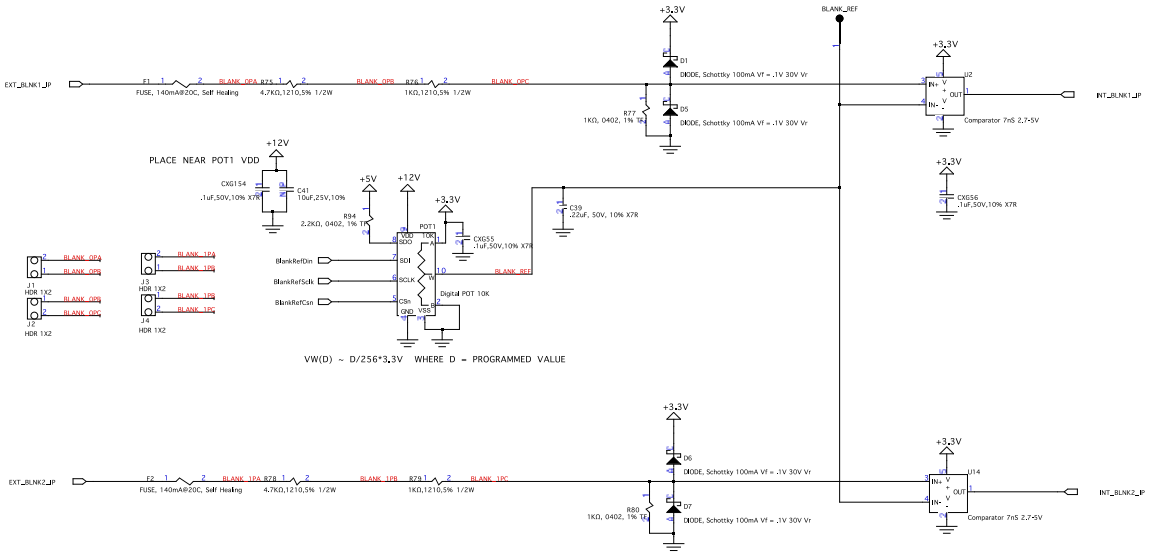
Headers and Shunts

VPX-GLIB has a number of options. Many of the options are software selectable and some require shunts used with headers.

Blanking

The Blanking inputs can be high or low voltage, single ended. As a result a comparator with several scaling resistor options and offset voltages are provided.

Page 12 of the schematic has the circuit.



Blanking Signal ⇔ FUSE ⇔ 4.7K ⇔ 1K comparator input with parallel 1K termination.

Series resistors are 1210 package, 1/2 W
The fuse is 140 mA rated
Each of the resistors is shuntable to take it out of the circuit.
Each of the signals is Diode coupled to +3.3 and Gnd to keep it within range of the comparitor.

BLANK1 uses J1 to isolate the 4.7K resistor – shunt to remove the resistor open to use the resistor. J2 isolates the series 1K. Install to remove, open to use.

BLANK2 uses J3 to isolate the 4.7K resistor – shunt to remove the resistor open to use the resistor. J4 isolates the series 1K. Install to remove, open to use.

Both shunts installed = 1K pull-down on blanking signal
4.7K installed [only 1K series in use] => 50% signal level seen by comparator
1K installed => ~17.5% signal level seen by comparator
neither installed => ~14.9% signal level seen by comparator

Recommended: Blanking <= 3.3V : both installed
3.3V < Blanking < 6.6V : use 1K shunt 4.7K
6.6V < Blanking < 18V use 4.7K shunt 1K
18V < Blanking < 22V use both, no shunts

Above 22V the diodes will pass current. Care must be taken to keep this below the maximum for the device including any temporary over-voltage situation [what the diode is really intended for]. A better solution for higher voltages would be to increase the series resistance.

The digital POT is programmed to select the switching point for the comparitor. Both Blanking signals use the same reference. The BLANK_REF test point is connected to the reference for ease of measurement. It is suggested to use a level near the mid point of the expected swing.

The signals are converted to LVTTL with the comparator and routed to the FPGA for further processing.

PCIe Clock selection

J6 is used to select between the local and RefClk generated PCIe clock. Open is the RefClk sourced PCIe clock and Shunted is the local crystal referenced version. It is recommended to use the RefClk [open] option if possible.

RefClk is used to create a 100 MHz PCIe reference clock. RefClk is 25 MHz and potentially has Spread Spectrum. The Clock generator is high quality Gen 1-4 rated. In addition the mux used to select between the two clock references is also rated Gen 1-4.

External Clock

The clock reference selected to drive the coax connector at the bezel has 2 options controlled by shunts. The output from the line driver passes through a resister divider [2.2K in series and in parallel] and then through a .022uF capacitor. J8 [resistor] and J7 [cap] can be installed to selectively remove the Series components.

When J8 is not installed the signal will be divided in half.
When J7 is not installed the signal will then be AC coupled.

The shunts are located near the coax connector at the bezel. The options are shown in the silk-screen.

Loop-back

VPX-GLIB uses the rear IO J2 connector, and 1 coax connectors for the IO. With PCIe8LSwVPX3U support VPX-GLIB J2 IO is accessible for loop-back.

A PMC BiSerial VI is used for loop-back tests and a complete solution.

Usually we list the loop-back connections in this section. Due to the extensive modifications to the BiSerial VI for the GLIB we have a separate document to capture the changes. Please contact Dynamic Engineering should you want to order a modified PMC-BiSerial-VI for your test station.

The loop-back apparatus supplies all of the external voltages to be measured, simulated fan inputs, complete SPI bus, matched opposites for the GPIO, LVDS/485 conversions and so forth. With Software and a special FLASH load on the BiSerial the GLIB is fully tested. We do use a scope to check the external 10 MHz delivered via the bezel coaz.

VPX P2 Rear IO

Name	Diff Pair #	Pin [P2]	Type
CAL_MOD_SW P	DP0	A1	LVDS
CAL_MOD_SW N	DP0	B1	
BLANK 0AP	DP1	D1	LVDS
BLANK 0AN	DP1	E1	
SPI CLK IN P	DP2	B2	LVDS
SPI CLK IN N	DP2	C2	
MOSI P	DP3	E2	LVDS
MOSI N	DP3	F2	
MISO P	DP4	A3	LVDS
MISO N	DP4	B3	
SPI DEV SEL 0 P	DP5	D3	LVDS
SPI DEV SEL 0 N	DP5	E3	
SPI DEV SEL 1 P	DP6	B4	LVDS
SPI DEV SEL 1 N	DP6	C4	
SPI DEV SEL 2 P	DP7	E4	LVDS
SPI DEV SEL 2 N	DP7	F4	
SPI DEV EN P	DP8	A5	LVDS
SPI DEV EN N	DP8	B5	
BLANK0 P	DP9	D5	LVDS
BLANK0 N	DP9	E5	
422_TO_PS P	DP10	D5	LVDS
422_TO_PS N	DP10	E5	
422_FRM_PS P	DP11	E6	
422_FRM_PS N	DP11	F6	
GPIO P	DP12	A7	LVDS
GPIO N	DP12	B7	
BLANK0B P	DP13	D7	LVDS
BLANK0B N	DP13	E7	
12VA	DP14	B8	Voltage
12VB	DP14	C8	Voltage
15VA	DP15	E8	Voltage
-15VA	DP15	F8	Voltage
15VB	DP16	A9	Voltage
12VC	DP16	B9	Voltage
8VA	DP17	D9	Voltage
5VA	DP17	E9	Voltage
-8VA	DP18	B10	Voltage
-15VB	DP18	C10	Voltage
15VC	DP19	E10	Voltage
12VD	DP19	F10	Voltage
EXT_422_TO_PS P	DP20	A11	485
EXT_422_TO_PS N	DP20	B11	
EXT_422_FRM_PS P	DP21	D11	485
EXT_422_FRM_PS N	DP21	E11	
FAN_1_TACH	DP22	B12	Sngl Ended
FAN_2_TACH	DP22	C12	Sngl Ended
FAN_3_TACH	DP23	E12	Sngl Ended

FAN_4_TACH	DP23	F12	Sngl Ended
EXT_CAL_OM_SW P	DP24	A13	485
EXT_CAL_OM_SW N	DP24	B13	
EXT_CAL_DF_SW P	DP25	D13	485
EXT_CAL_DF_SW N	DP25	E13	
TMP_DX P	DP26	B14	3906 emitter
TMP_DX N	DP26	C14	3906 base
EXT_CAL_MOD_SW	DP27	E14	LVTTL
GND	DP27	F14	
BLANK1 P	DP28	A15	LVDS
BLANK1 N	DP28	B15	
SPARE	DP29	D15	
SPARE	DP29	E15	
EXT_BLNK1_IP	DP30	B16	Sngl Ended
EXT_BLNK2_IP	DP30	C16	Sngl Ended
EXT10MHZ	DP31	E16	+7 dbm
EXT-GPIO	DP31	F16	LVTTL

FIGURE 2 VPX GLIB P2 PIN ASSIGNMENT

Sngl Ended signals in the case of Blanking can be various voltages and the GLIB features for scaling should be used for proper operation. For the FAN inputs, the LM81 datasheet can be referenced, standard FAN inputs are generally acceptable. Diagrams and voltage ranges are documented in the data sheet.

Front Panel Clock Interface Pin Assignment

Name	Pin [J5]
10 MHZ	center conductor

FIGURE 3 VPX GLIB FP CLK J5 PIN ASSIGNMENT

J5 is SSMC connectors with 10 MHz available. The signal is driven with TTL levels [24 mA +/-]. Two shunt options are available to add or subtract the series resistor and capacitor. The Series resistor is 2.2K. The parallel termination to ground is also 2.2K allowing the signal to be divided in half. The capacitor is .022 uF and can provide AC coupling. Install J7 for DC coupling and open for AC. Install J8 for full power and open for ½ signal voltage. See silk-screen near bezel / coax connector.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
VPX-GLIB is a 3U 4 HP card meant to be installed into a VPX chassis. VPX-GLIB is fitted with guide pins which aide in alignment prior to mating the VPX connectors. The VPX connectors are blade style and make high quality connections with reasonable insertion pressure required.

VPX-GLIB has an internal thermal plane connected to the locations where standard wedge lock hardware can be installed. The wedgelocks are an option. Consult your chassis documentation to see if your system needs wedgelocks or standard card guides. When wedgelocks are installed the bezel is not installed in favor of a chassis level cover.

Install with the power off. Be sure to properly install the card – the bezel should be fully seated on the chassis mounting rail.

It is recommended to use the handle lock to fully seat and lock the card into place.

Attach the coax clock reference cable if used.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the VPX GLIB when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time.

Construction and Reliability

VPX GLIB is constructed out of 0.062 high temp ROHS compliant material. Gold has been used for plating rather than Tin for improved performance over time. “leaded or unleaded” components can be used along with solder choices. Dynamic Engineering can support both processes.

Surface mounted components are used. The connectors are through hole soldered for the cables and compression fit for the VPX.

Thermal Considerations

The VPX GLIB is built with “industrial” parts. -40 ⇔ 80 C or better.

The base design is fairly low powered and will not require a lot of cooling. External draw on the power supplies or IO signals can add a significant power load on GLIB. Forced air cooling is recommended in this case.

During T&I it is recommended to read the temperature sensor and see what temperature is registering on the board. If anywhere close to 70C forced air should be implemented. The MTBF will be longer at cooler temperatures [up to a point]. Remember that the LM81 is measuring the temperature on the FAB near the FPGA. Other parts may be warmer and likely are hotter than the surface temperature of the PCB. Getting the temperature reading below 50C will provide quite a bit of margin and add to the MTBF.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

https://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite B&C
Santa Cruz, CA 95060
831-457-8891
InterNet Address support@dyneng.com

Specifications

CLK rates supported:	10 MHz from rear panel or local osc, 10 MHz [LVTTL] on SSMC
Power	local supplies for internal requirements based on +5, 3.3 and 12 from VPX bus.
SPI / PCIe	Internal SPI used directly or converted to SMB. Registers are accessible from SPI. PCIe access in parallel with SPI control.
IO	Additional miscellaneous and program specific IO are supported with a combination of RS-485, LVTTL, LVDS, and IO specific voltage inputs.
Monitor	Three LM81s are supplied along with an SMB interface to measure the temperature, the local voltages, various external voltages, and fan speeds. In addition a TMP422 is supplied to support remote temperature determination.
FLASH	FPGA program is stored into FLASH memory via the defined JTAG connections on P0.
Software Interface:	register mapped IO
Initialization:	registers are initialized to 0.
Interface:	Registers are generally R/W with the exception of Status bits.
Dimensions:	3U 4HP
Construction:	High Temp ROHS compliant Multi-Layer Printed Circuit board, Through Hole and Surface Mount Components. Standard processing with leaded components and solder. – ROHS option for ROHS compliant components and solder.

Order Information

extended temperature range –40 ⇔ +85C

VPX-GLIB	3U 4HP VPX card Temperature & Voltage Monitor, Fan Monitor High voltage “blanking” interface, SPI control, Clock reference, Extended Temp is standard on this model https://www.dyneng.com/VPX-GLIB .html
-ROHS	Add for ROHS processing.
-CC	Add for Conformal Coating