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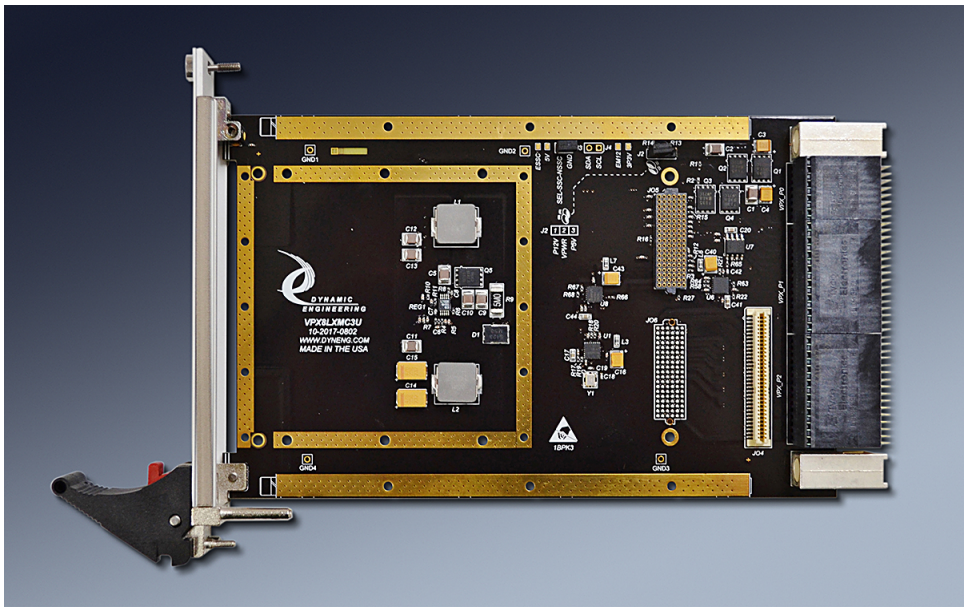
User Manual

VPX8LXMC3U

VPX 8 Lane XMC 3U Compatible Carrier



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VPX8LXMC3U
VPX and XMC Compatible Carrier

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The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Connection of incompatible hardware is likely to cause serious damage.

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Product Description

VPX8LXMC3U is part of the Dynamic Engineering VPX and XMC compatible family of modular I/O components. VPX8LXMC3U adapts a XMC device to a 3U VPX device.

VPX8LXMC3U supports 8 PCIe lanes for data communication and provides either a Spread Spectrum Clock (SSC) or Non Spread Spectrum Clock (NSSC) to the XMC device. Both the SSC and NSSC are PCIe Gen1 through Gen3 compliant.

Two separate clock generator devices are used to generate a SSC and a NSSC. A PCIe Gen1 through Gen3 compliant clock multiplexor is used to select which clock is provided to the XMC device.

One clock generator uses the VITA 25 MHz SSC REF_CLK input to generate the 100MHz SSC. The other uses using a 25MHz crystal output as an input to generate the 100MHz NSSC.

Extended testing has been performed on the VPX8LXMC3U in both modes (SSC and NSSC) using the PCIe8LSwVPX3U and an installed XMC-Parallel-TTL. DMA operations were run overnight multiple times in both modes without failure and no TLP corrections required at the switch (on the PCIe8LSwVPX3U).

XMC VPWR can be either +5V or +12V and is selectable via a header. VPWR is routed using low impedance high amperage rated FET's. More than 10A can be supplied to VPWR assuming adequate 5V or 12V input power.

An board power converter uses 12V to generate and supply -12V to the XMC connector

In addition to the 8 PCIe lanes, 32 differential user IO signals are routed between the VPX and XMC connectors. All of the differential pairs are routed with controlled impedance and matched length.

VPX8LXMC3U is designed with an option for wedgelock hardware to be added. A special internal thermal plane is tied to the wedgelock pads as well as the heatframe for the XMC. This option is ordered with –CC1 for the HeatFrame, and –CC2 for the wedgelocks. When ordering with –CC1 the standard bezel with XMC cutout is replaced with a blank version since rear IO is used with ccXMC models.

Special features:
• 1-8 lane PCIe interface
• PCIe Gen1 through Gen3 SSC compliant clock generator using VITA REF_CLK
• PCIe Gen1 through Gen3 NSSC compliant clock generator
• Selectable VPWR - can be either +5V or +12V
• 32 differential IO pairs – to/from VPX / XMC connectors
• Differential pair routing - length matching and impedance control
• I2C connectivity to XMC device via I2C header
• JTAG signaling from VPX carrier to XMC.

VPX8LXMC3U is ready to use. Just install an XMC card onto the VPX8LXMC3U and then onto a system interface board such as the PCIe8LSwVPX3U.

VPX8LXMC3U Architecture

Figure 1 provides an architectural view of VPX8LXMC3U. VPX8LXMC3U provides bridging between VPX and XMC devices. Using a header (J2) it can be configured to provide either 12V or 5V to the XMC VPWR connector pins. A 12V to -12V power conversion circuit is also provided to supply the XMC device with -12V. PCIe Gen1-Gen3 compliant NSSC and SSC clock circuits provide two different clocking options. 8 lanes of PCIe and 32 pairs of user IO differential signaling are provided.

VPX8LXMC3U Block Diagram

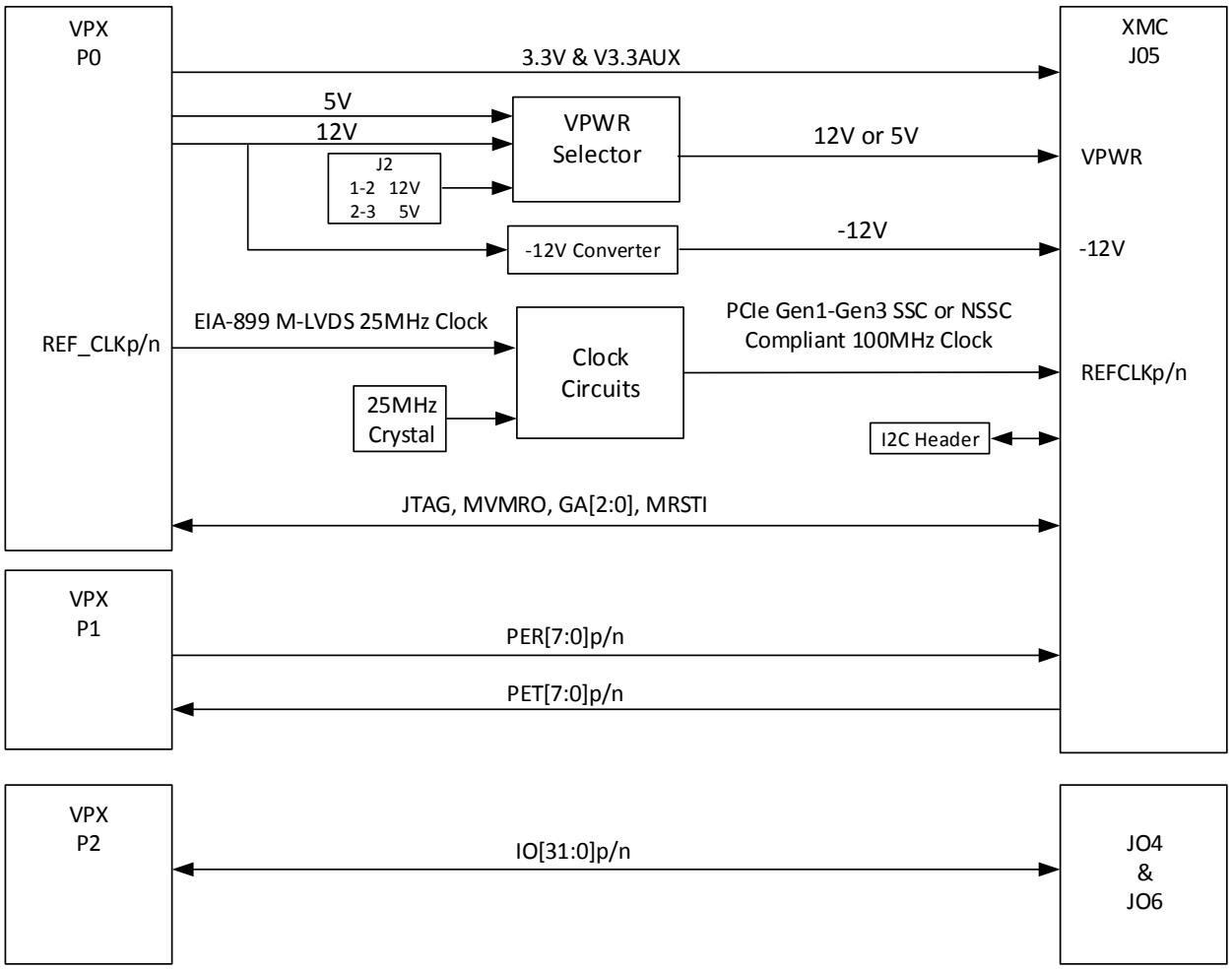

FIGURE 1 VPX8LXMC3U BLOCK DIAGRAM

VPX8LXMC3U Clocking

VPX8LXMC3U supports both PCI Express Independent Non-Spread Spectrum Clocking (NSSC) and VITA Spread Spectrum Clocking (SSC). Figure 2 is a block diagram of the VPX8LXMC clocking architecture. The clocking selected is configured before power on using a two pin header (J3). When the header is left open VITA SSC is selected. When a jumper is installed on J3 NSSC is selected. In either case the clock provided to the XMC device is PCIe Gen1-Gen3 compliant.

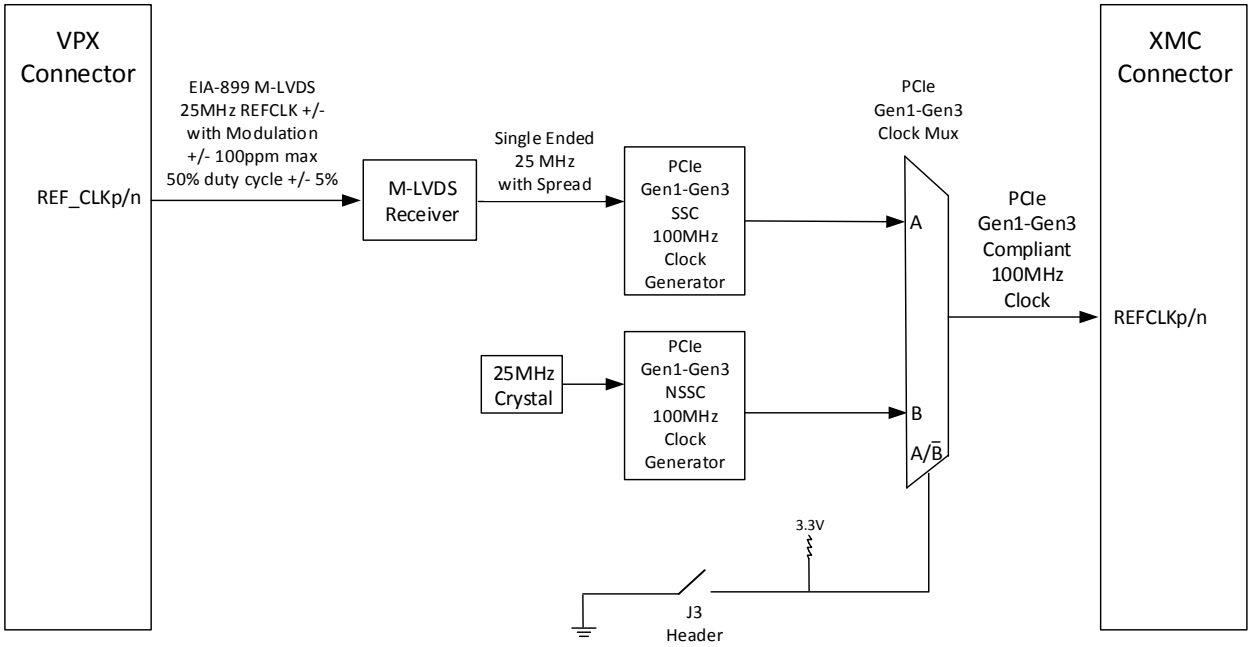

FIGURE 2 VPX8LXMC3U CLOCKING

VPX8LXMC3U Clocking – System View

The VPX standard does not support the PCIe reference clock, but does support PCIe independent Non Spread Spectrum Clocking (NSSC) and Spread Spectrum Clocking (SSC) using a lower frequency common (25MHz) REF_CLK. A VPX device needs to provide a local reference clock. Dynamic Engineering's PCIeLSwVPX3U with the VPX8LXMC3U (figure 3) provides an example of both clocking implementations.

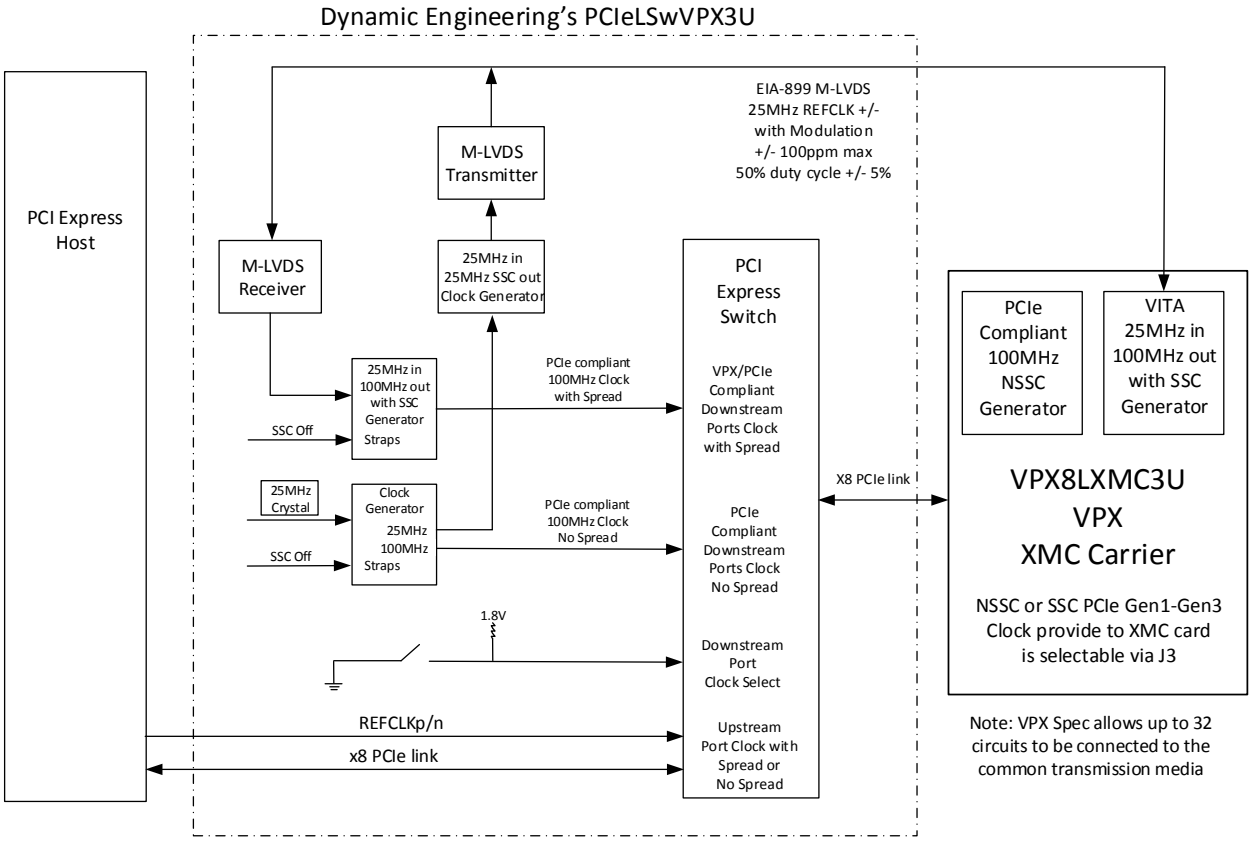

FIGURE 3 VPX8LXMC3U CLOCKING – SYSTEM VIEW

The PCIe Switch isolates the upstream PCIe reference clock (which can be either a NSSC or SSC) from the VPX side. The PCIe Switch's 8 lane downstream port communicates with the VPX device, and can be configured to operate with either a NSSC or with the SSC generated from the common VITA spec'd 25 MHz SSC (REF_CLK+/-)

Headers and TestPoints

J2 VPWR select, 1-2 selects 12V and 2-3 selects 5V on VPWR pins.

J3 Clock select, 1-2 open selects SSC and 1-2 shunted selects NSSC.

J4 I2C header, provides access to XMC I2C port/pins. 1 is clock, 2 is data.

ESSC Test pad to view Single Ended 25MHz VITA SSC REF_CLKp/n.

5V, EM12, 3P3V pads to measure voltages.

VPX Module Backplane IO Interface Pin Assignment

Figure 4 gives the pin assignments for the VPX Module IO Interface – from VPX J2 [Backplane] to VPX8LXMC3U P2 [this adapter] to the VPX8LXMC3U XMC JO4 and JO6 connectors. DE_NET is the schematic net name that connects P2 signals to JO4 and JO6 on the VPX8LXMC3U schematic. J2 is provided as a reference due to the pin translation within the P2/J2 pair. Please see the User Manual for your XMC board for more information.

VPX J2 ⇔ VPX P2 ⇔ XMC JO4 & JO6

VPX[J2]		VPX [P2]		XMC[JO4]		XMC[JO6]		DE_NET_NAME	
P	N	P	N	P	N	P	N		
G16	H16	E16	F16	62	64	D19	E19	IO1_31P	N
C16	D16	B16	C16	61	63	A19	B19	IO1_30P	N
E15	F15	D15	E15	58	60	D17	E17	IO1_29P	N
A15	B15	A15	B15	57	59	A17	B17	IO1_28P	N
G14	H14	E14	F14	54	56	D15	E15	IO1_27P	N
C14	D14	B14	C14	53	55	A15	B15	IO1_26P	N
E13	F13	D13	E13	50	52	D13	E13	IO1_25P	N
A13	B13	A13	B13	49	51	A13	B13	IO1_24P	N
G12	H12	E12	F12	46	48	F11	F12	IO1_23P	N
C12	D12	B12	C12	45	47	C11	C12	IO1_22P	N
E11	F11	D11	E11	42	44	D11	E11	IO1_21P	N
A11	B11	A11	B11	41	43	A11	B11	IO1_20P	N
G10	H10	E10	F10	38	40	F9	F10	IO1_19P	N
C10	D10	B10	C10	37	39	C9	C10	IO1_18P	N
E9	F9	D9	E9	34	36	D9	E9	IO1_17P	N
A9	B9	A9	B9	33	35	A9	B9	IO1_16P	N
G8	H8	E8	F8	30	32	F7	F8	IO1_15P	N
C8	D8	B8	C8	29	31	C7	C8	IO1_14P	N
E7	F7	D7	E7	26	28	D7	E7	IO1_13P	N
A7	B7	A7	B7	25	27	A7	B7	IO1_12P	N
G6	H6	E6	F6	22	24	F5	F6	IO1_11P	N
C6	D6	B6	C6	21	23	C5	C6	IO1_10P	N
E5	F5	D5	E5	18	20	D5	E5	IO1_9P	N
A5	B5	A5	B5	17	19	A5	B5	IO1_8P	N
G4	H4	E4	F4	14	16	F3	F4	IO1_7P	N
C4	D4	B4	C4	13	15	C3	C4	IO1_6P	N
E3	F3	D3	E3	10	12	D3	E3	IO1_5P	N
A3	B3	A3	B3	9	11	A3	B3	IO1_4P	N
G2	H2	E2	F2	6	8	E1	F2	IO1_3P	N
C2	D2	B2	C2	5	7	C1	C2	IO1_2P	N
E1	F1	D1	E1	2	4	D1	E1	IO1_1P	N
A1	B1	A1	B1	1	3	A1	B1	IO1_0P	N

FIGURE 4 VPX8LXMC3U VPXJ2/P2-XMCJO4JO6

J06.D19 is connected to J04.62 is connected to P2.E16 which becomes J2.G16

Figure 5 provides the VPX P1 (VPX8LXMC3U) and J1 (backplane) connector pin locations.

VPX Module P1/J1 PCIe lane assignments

Signal		P1		J1	
LN0-RX+	LN0-RX-	A1	B1	A1	B1
LN0-TX+	LN0-TX-	D1	E1	E1	F1
LN1-RX+	LN1-RX-	B2	C2	C2	D2
LN1-TX+	LN1-TX-	E2	F2	G2	H2
LN2-RX+	LN2-RX-	A3	B3	A3	B3
LN2-TX+	LN2-TX-	D3	E3	E3	F3
LN3-RX+	LN3-RX-	B4	C4	C4	D4
LN3-TX+	LN3-TX-	E4	F4	G4	H4
LN4-RX+	LN4-RX-	A5	B5	A5	B5
LN4-TX+	LN4-TX-	D5	E5	E5	F5
LN5-RX+	LN5-RX-	B6	C6	C6	D6
LN5-TX+	LN5-TX-	E6	F6	G6	H6
LN6-RX+	LN6-RX-	A7	B7	A7	B7
LN6-TX+	LN6-TX-	D7	E7	E7	F7
LN7-RX+	LN7-RX-	B8	C8	C8	D8
LN7-TX+	LN7-TX-	E8	F8	G8	H8

FIGURE 5 VPX8LXMC3U PCIE/VPXP1/J1

Please note: (1) VPX definitions are relative to VPX. PCIe connector definitions are relative to the PCIe bus. (2) VPX standard does not support the PCIe reference clock, but does support independent clocking and SSC using a lower frequency REF_CLK. It is expected the VPX will provide a local reference clock 3. PCIe lanes are routed to XMC J05.

VPX Module J0/P0 Power/Signal assignments

Signal	J0
GND	A4, A5, A6, A8, B8, C7, D4, D5, D6, D7, E8, F4, F5, F6, F8, G7, H7, I4, I5, I6, I8
12V	F1, F2, G1, G2, H1, H2, I1, I2
3.3V	A1, A2, B1, B2, C1, C2, D1, D2
5V	A3, B3, C3, D3, F3, G3, H3, I3
3.3V AUX	E5
M12 AUX	OPEN
P12AUX	OPEN
GAP	H5
GA[4:0]	G5, H6, G6, C6, B6
TDO	F7
TDI	E7
TRST#	A7
TMS	B7
TCK	I7
PERST#	C4

Signal	P0
GND	A8, C4, C5, C6, C7, D8, E4, E5, E6, F7, G8, F4, F5, F6, F8, G7, H7, I4, I5, I6, I8
12V	E1, E2, F1, F2, G1, G2, I1, I2
3.3V	A1, A2, B1, B2, C1, C2, D1, D2
5V	A3, B3, C3, E3, F3, G3, H3, I3
3.3V AUX	D5
M12 AUX	OPEN
P12AUX	OPEN
GAP	G5
GA[4:0]	F5, G6, F6, B6, A6
TDO	E7
TDI	D7
TRST#	A7
TMS	B7
TCK	G7
PERST#	B4

FIGURE 6 VPX8LXMC3U POWER P0/J0

Note: 3.3V Aux is routed to XMC 3.3V Aux and will be powered from VPX power supply as defined by your system. PERST# is the PCIe reset signal and is routed to the XMC J05.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
Typically the XMC device is mounted onto the VPX8LXMC3U prior to plugging it into a VPX slot/location or a PCIe VPX 3U Compatible Carrier such as Dynamic Engineering's PCIe8LSwVPX3U which is then installed within the Host system chassis. The VPX8LXMC3U is fitted with VPX compliant mounting / alignment receptacles. P0 is toward the top of the card. The alignment receptacles are offset to provide keying to prevent improper card installation. Rocking the VPX slightly during installation can help with the process of installation. The blades have proven to be quite robust, however; the connectors are expensive so be careful.

VPX8LXMC3U can be mounted in air-cooled VPX3U chassis with standard card guides for an .062" thick board. A conduction cooled chassis can be used when the –CC1 and –CC2 options are added for wedgelocks and heatframe.

JTAG access to the XMC is accomplished through the VPX carrier as there is no JTAG header on the VPX8LXMC3U. I2C access to an XMC device can be achieved using the J3 header on the VPX8LXMC3U.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI/PCIe devices found at boot up on a "splash screen" with the VendorID and CardId for the VPX installed and an interrupt level. If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltages to the VPX8LXMC3U when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the XMC installed onto the VPX8LXMC3U than the VPX8LXMC3U itself, and it is smart system design when it can be achieved.

Construction and Reliability

VPX8LXMC3U is constructed out of 0.062 inch thick high temp RoHS compliant FR4 material. The components on VPX8LXMC3U are tied into the internal power planes to spread the dissipated heat out over a larger area. This is an effective cooling technique in the situation where a large portion of the board has little or no power dissipation. In addition the thermal plane [2 oz] covers the board and is tied to the heat frame and wedge lock locations. Even when not in direct use the thermal plane will help spread any thermal load from the XMC.

The VPX Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. The current rating varies with the blade type. At the moment Tyco is the only vendor providing VPX connectors.

Thermal Considerations

If the XMC installed has a large heat dissipation; forced air cooling is recommended.

VITA Multipoint SSC Clocking implementation

The VITA Specification defines, and the VPX8LXMC3U circuits support the VITA maximum of 32 circuits connected together on a common transmission media.

The VPX8LXMC3U supports the VITA Multipoint SSC specification by using the common 25MHz VITA SSC that is transmitted and received using M-LVDS differential transceivers. The VPX8LXMC3U can be configured to use the VITA 25MHz SSC to generate and supply the XMC device with a 100MHz Gen1-Gen3 compliant SSC clock.

Dynamic Engineering has validated the VPX8LXMC3U VITA 25MHz SSC clocking design using Dynamic Engineering's PCIe8LSwVPX3U (also supports VITA SSC clocking) and the XMC-PARALLEL-TTL board. Figure 5 shows the maximum configuration of 32 circuits connected together.

PCIe8LSwVPX3U VITA System Clocking – Maximum Configuration

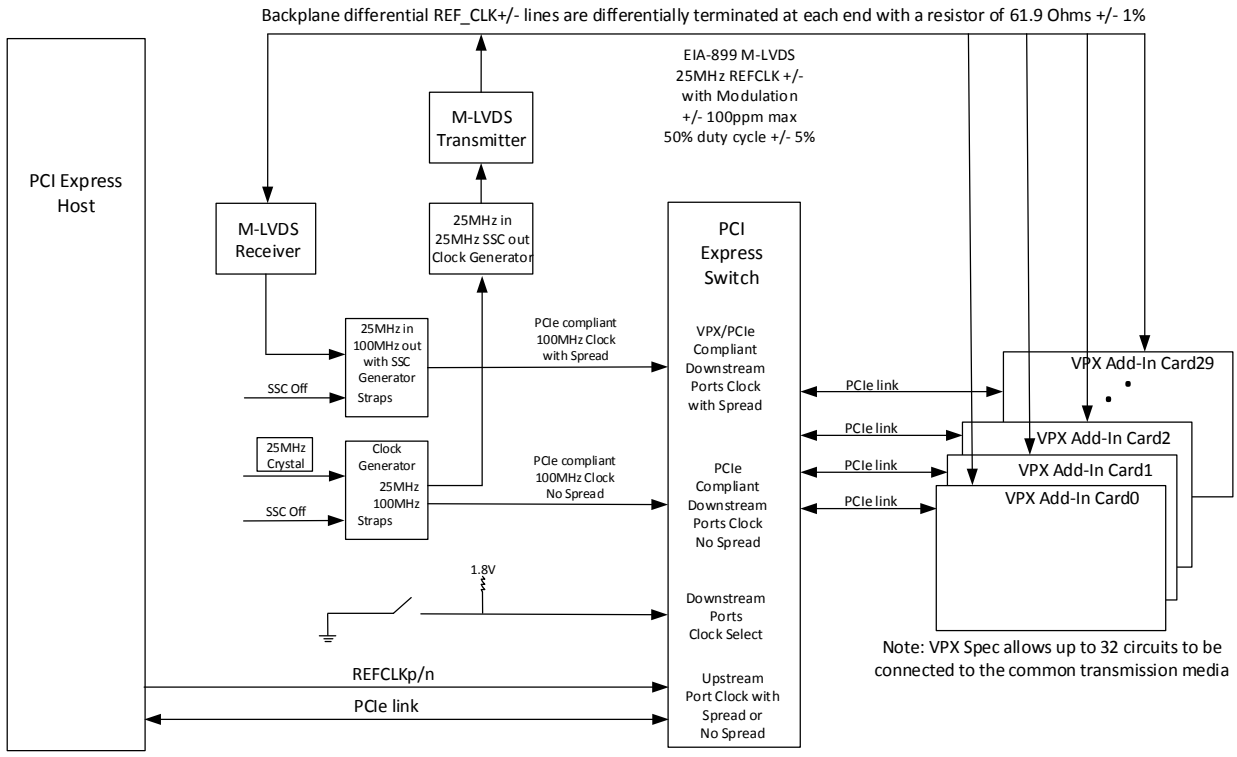

FIGURE 7 VITA SYSTEM CLOCKING – MAXIMUM CONFIGURATION

Loopback Testing

For Engineering and Production test of VPX8LXMC3U, Dynamic Engineering uses PCIe8LSwVPX3U, XMC-PARALLEL-TTL, and a loopback fixture to test it. Figure 7 shows the validation and ATP test configuration.

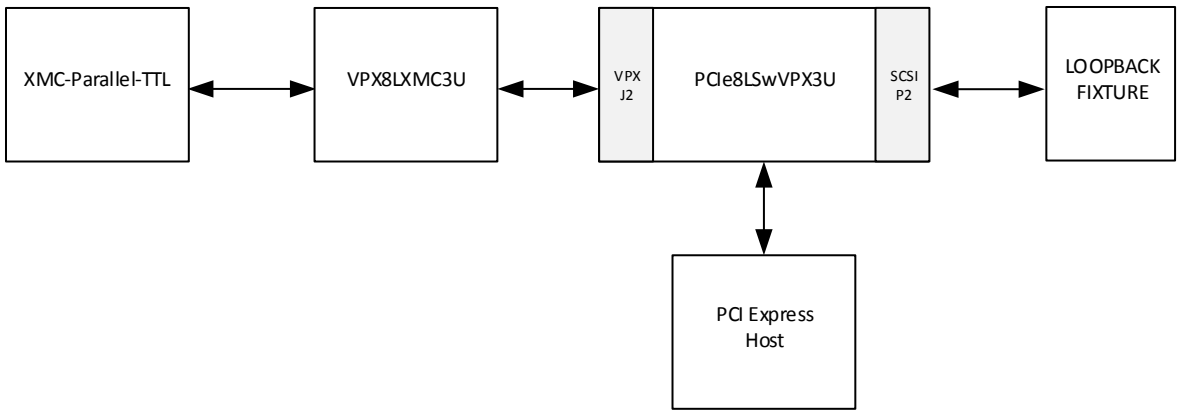

FIGURE 8 VPX8LXMC3U LOOPBACK TEST CONFIGURATION

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
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Specifications

Logic Interfaces:	PCIe 1- 8 lanes per VPX/XMC
Access types:	All modes supported.
CLK rates supported:	Gen1, Gen2, Gen 3
Software Interface:	Transparent design with no software required for adapter. Installed XMC will determine control of that device.
Initialization:	Global Addressing if needed.
Interface:	VPX P0, P1, P2 to XMC JO5 & JO4/JO6
Dimensions:	VPX 3U 4HP
Construction:	High Temp FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.

Order Information

standard temperature range -40⇔85ºC

VPX8LXMC3U	VPX 3U 4HP with single XMC position http://www.dyneng.com/VPX8LXMC3U.html
-ROHS	ROHS compliant parts and process
-HF1	Add heatframe to board for conduction cooled XMC
-HF2	Add wedgelocks to VPX8LXMC3U for conduction cooled chassis support. This option removes bezel.
-CC	Add conformal coating
HDEterm68	http://www.dyneng.com/HDEterm68.html 68 pin SCSI II to 68 screw terminal converter with DIN rail mounting.
HDEcabl68	http://www.dyneng.com/HDEcabl68.html SCSI cables with latch blocks or thumbscrews and various lengths are available. Custom lengths can be ordered.
PCIe8LSwVPX3U	VPX adapter into PC. 1-8 lanes. Switch based to allow both SSC and NSSC operation of VPX adapter. Rear IO routed through to SCSI connector at bezel. Useful debugging aide for developing SW and HW in a PC environment. http://www.dyneng.com/PCIe8LSwVPX3U.html