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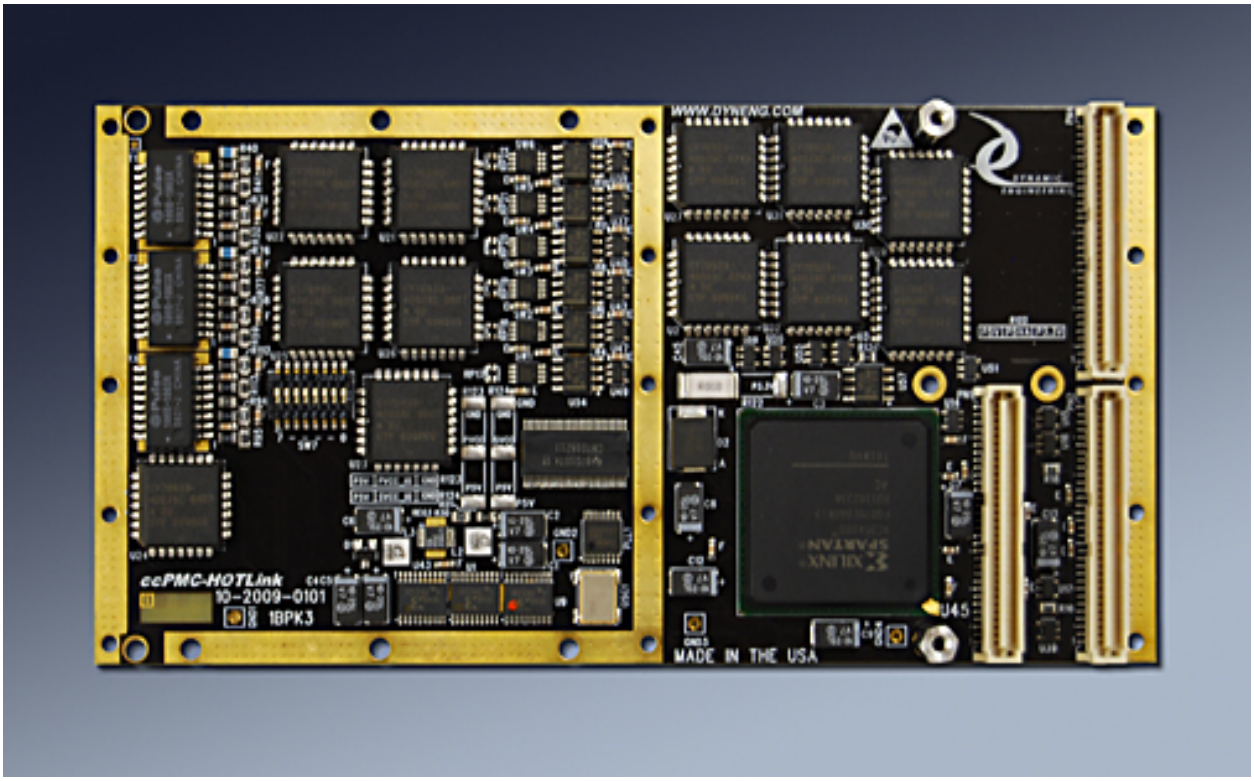
Est. 1988

User Manual

ccPMC-HOTLink-Kaon1

Conduction-Cooled
Two-Channel HOTLink® Interface



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ccPMC-HOTLink-Kaon1
2-Channel HOTLink® Interface
Conduction-Cooled PMC Module

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Connection of incompatible hardware is likely to cause serious damage.

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Product Description

The ccPMC-HOTLink is part of the PMC Module family of modular I/O components by Dynamic Engineering. It features the Cypress Semiconductor CY7B923/CY7B933 HOTLink® Transmitter/Receiver pair. The HOTLink protocol implemented provides positive emitter-coupled logic (PECL) data inputs and outputs. The transmit byte-rate is determined by the programmed frequency of the PLL, which is programmed by software over a serial I2C interface. The PLL clock A output is used for the HOTLink interface. The PLL frequency is multiplied ten times by the HOTLink transmitter to send the transmit byte data-stream which is expanded to 10 bits by the internal 8B/10B encoder. Six independent HOTLink channels are laid-out per card. Each HOTLink channel has four differential I/O signal pairs: A HOTLink differential PECL output, a HOTLink differential PECL input and two bi-directional differential RS-485 lines. See the standard configuration block diagram below:

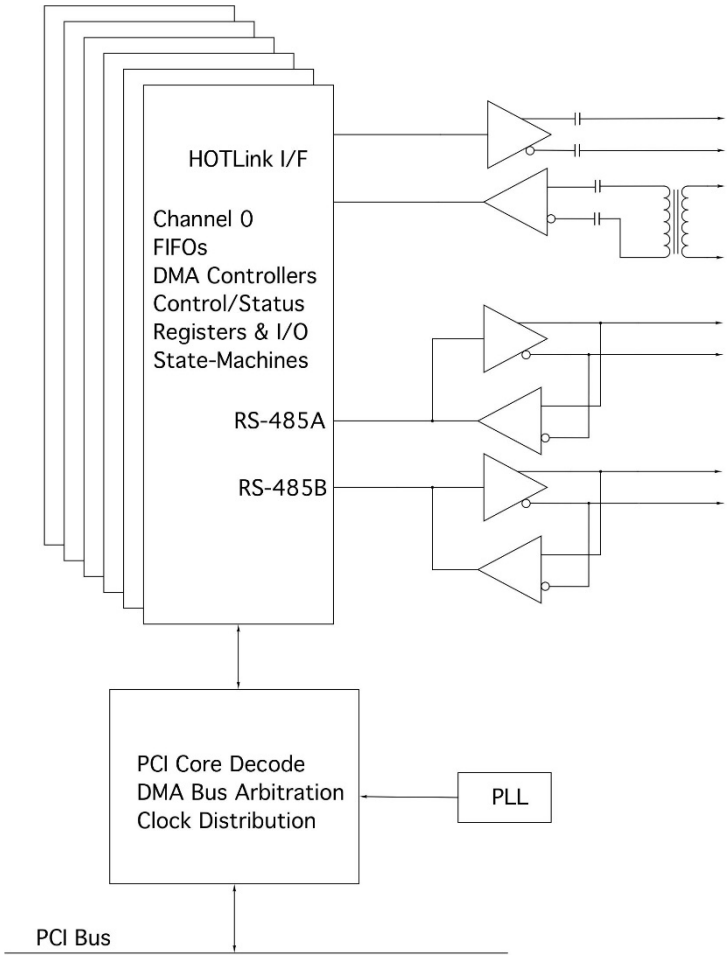


FIGURE 1 CCPMC-HOTLINK BLOCK DIAGRAM

The ccPMC-HOTLink-Kaon1 is a custom version that has only two channels installed with no RS-485 lines. Each channel has a HOTLink differential PECL output, a HOTLink differential PECL input, one AC coupled TTL output and one input. The differential HOTLink input connects to dual 50 Ω terminations referenced to 1.8 volts. The signals are then AC-coupled into the HOTLink receiver inputs referenced to 3.5 volts. The HOTLink output is AC-coupled after the bias/termination network.

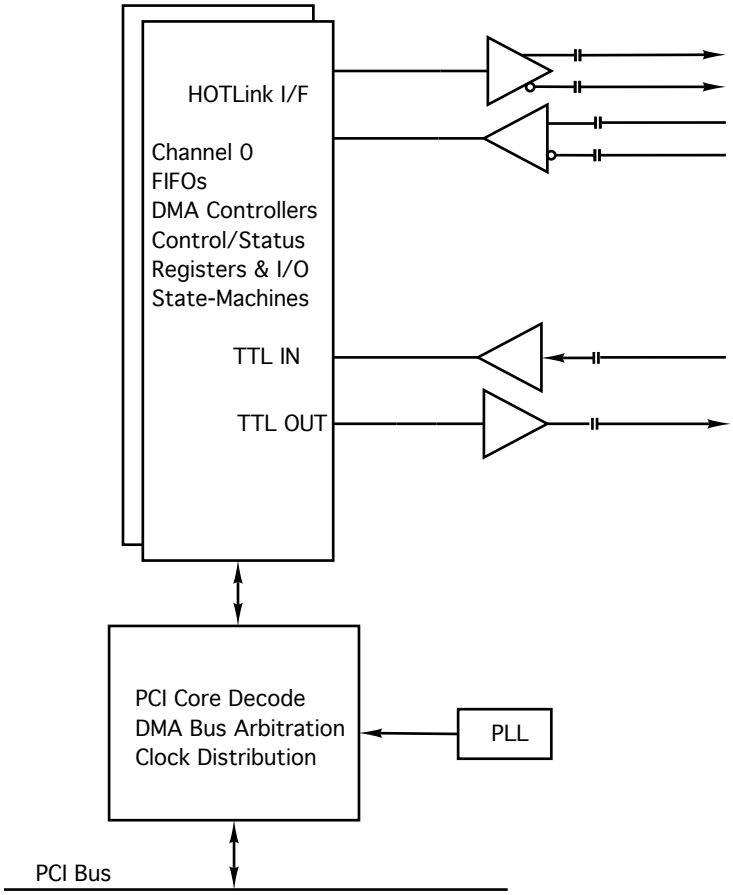


FIGURE 2 CCPMC-HOTLINK-KAON1 BLOCK DIAGRAM

The HOTLink receivers are supported by 32k by 32-bit input data FIFOs and the HOTLink transmitters have 32k by 32-bit output data FIFOs. These FIFOs can be accessed by single-word read/writes as well as DMA burst transfers. A FIFO test bit in each channel control register enables the data to be automatically routed from the transmitter FIFO output to the receiver FIFO input for a full 32-bit path for loop-back testing of the FIFOs. Data is latched and the bus immediately released on a write-cycle, and as soon as data is present in the receive FIFO, it is pre-read to be immediately available for a read cycle. This allows minimal delay on the PCI write to transmitter FIFO path and PCI read from the receiver FIFO path.

There is also a 128-word by 32-bit dual-port RAM for each channel. This RAM is used to store format information for the HOTLink transmitter to break the transmitted data in groups with control characters delimiting the data-blocks. During board testing the format RAM is also used by the receiver to verify the format of received data.

Each channel also has an output and input TTL line running a custom synchronous 32-bit LSB first protocol. Each line is supported by 4k by 32-bit FIFOs which are accessed using single-word read/writes. A FIFO test bit in the TTL control register enables the data to be automatically routed from the transmitter FIFO output to the receiver FIFO input for a full 32-bit path for FIFO loop-back testing. A TTL trigger enable bit in the channel control register enables the TTL receiver to send requests to the HOTLink transmitter state-machine. These requests trigger the output of a block of data from the HOTLink transmitter.

The received HOTLink data is written as long-words to the receive FIFO. The first byte received is loaded into byte position zero (bits 7-0), the second byte goes in byte one (bits 15-8) and so on. If the receiver is disabled when a long-word has not been completed, the remaining unfilled bytes are set to zeros and the long-word is written to the receive FIFO.

Similarly the HOTLink transmitter reads long-words from the transmit FIFO and sends byte zero first followed by byte one, byte two and finally byte three.

The ccPMC-HOTLink-Kaon1 board supports multiple interrupts. An interrupt can be configured to occur when the transmit FIFO is almost empty or the receive FIFO is almost full as well as other events and error conditions. All interrupts are individually maskable and a channel master interrupt enable is provided to disable all interrupts on a channel simultaneously. The current real-time status is also available making it possible to operate in a polled mode.

This PMC module is conduction-cooled and has no front panel connector. All I/O connections are routed through PN4 and the PMC carrier to the outside world.

ccPMC-HOTLink conforms to the PMC and CMC standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

ccPMC-HOTLink uses a 10 mm inter-board spacing for the standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

Theory of Operation

ccPMC-HOTLink-Kaon1 board features a Spartan6-100 Xilinx FPGA. The FPGA contains the PCI interface, all of the registers, FIFOs, RAM and protocol controlling elements of the Kaon1 HOTLink design. Only the, HOTLink transmitter and receiver, input and output TTL drivers, FPGA configuration flash memory and clock circuitry are external to the Xilinx device.

ccPMC-HOTLink-Kaon1 board is designed to interface with an existing legacy system. A 60-byte data block, preceded by a two-cycle start-bit is sent to the TTL input line to initiate the transfer of HOTLink data. The format of the HOTLink data is defined by the contents of a 128-byte RAM block in the FPGA. The first two bytes of the format RAM contain the total byte-count of the transmitted data-frame. The subsequent bytes represent framing control characters. After an arbitrary number of control characters, a 0xFF byte signals the start of a data block. The byte after the 0xFF indicates the number of data-bytes in the referenced data-block. After the data block, subsequent bytes once again represent framing control characters until another 0xFF is seen signifying another data-block, whose byte-count is contained in the byte after the 0xFF. The data to be sent is read from the transmitter data-FIFO and interleaved with the format control bytes. This process continues until NULL characters (0x05) are read from the format RAM which indicates the end of the data-frame.

After the 60 bytes of TTL data (960 cycles), 2110 cycles of NULL information (1055 zeros) are input to the TTL receiver. The whole process repeats until the system is disabled. Each TTL bit consists of two clock cycles. A ‘0’ is represented by two 50% duty cycle clock cycles. A ‘1’ is represented by a 25%/75% duty cycle clock followed by a 75%/25% duty cycle clock. See figure 3 below which shows a “100011” encoded:

FIGURE 3 CCPMC-HOTLINK-KAON1 TTL BIT FORMAT

Scatter-gather bus-master DMA is provided in this design. Once the physical address of the first chaining descriptor is written to the DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the IO buffer passed to the read or write call. The next four bytes comprise a long-word indicating the length of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is set to one if the IO transfer is from the ccPMC-HOTLink-Kaon1 board to host memory, and zero if the transfer is from host memory into the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one. This process continues automatically

until the last chaining descriptor in the list is processed. The channel's input and output DMA engines interface with the HOTLink transmit and receive FIFOs while the two TTL FIFOs are accessed by single-word transfers only.

In normal operation, a command is received by the channel's TTL line about once every 446 microseconds (see Figure 4 below). In response to this command ccPMC-HOTLink-Kaon1 sends a frame of high-speed serial data at a rate of 167.77 Mbits/second (see Figure 4 below). This data has 8B/10B encoding with differential PECL signal levels.

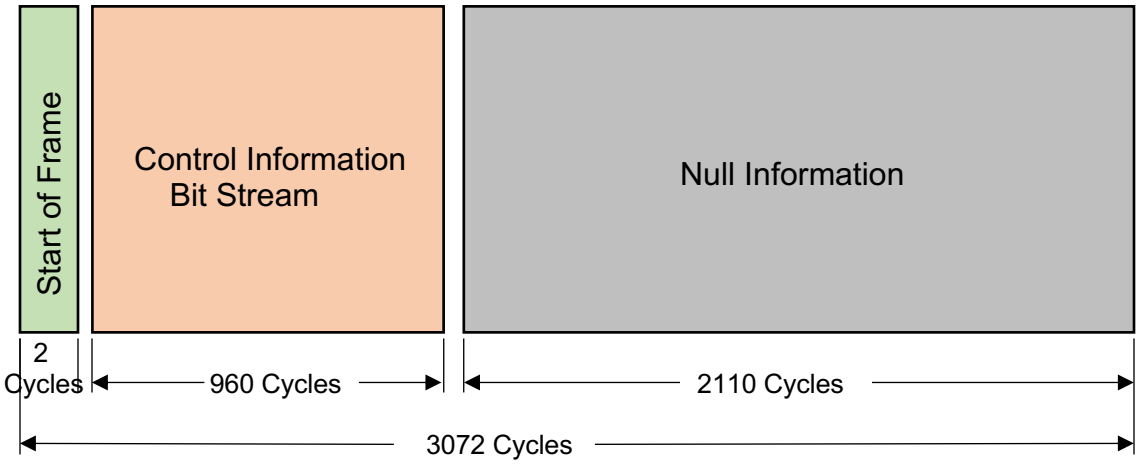


FIGURE 4 CCPMC-HOTLINK-KAON1 TTL DATA-BLOCK FORMAT

Each ccPMC-HOTLink-Kaon1 channel also has an onboard HOTLink receiver. The receiver is present for test purposes and is connected to the transmitter always-on output C by an internal link to receiver input B. Receiver input A is AC-coupled to Pn4 for an external loop-back test connection to transmitter output A.

Programming

Programming ccPMC-HOTLink-Kaon1 board requires the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the board is installed. The VendorId = 0xDCBA. The CardId = 0x0064.

Depending on the software environment it may be necessary to set-up the system software with the ccPMC-HOTLink-Kaon1 "registration" data. If DMA is to be used it will be necessary to acquire a block of non-paged memory that is accessible from the PCI bus in which to store chaining descriptor list entries. If the Dynamic Engineering device driver is used, the driver will handle all the DMA internal mechanics automatically.

In order to transmit or receive either HOTLink® or TTL data, the PLL must be programmed to the desired clock configuration. The PLL is connected to the Xilinx by an I^2C serial bus and its internal registers are loaded with 40 bytes of data that can be derived from a .jed file generated by the CyberClock utility from Cypress semiconductor https://www.dyneng.com/CyberClocks.zip. Open the utility and select CY22393 under the CyClocksRT menu. The reference frequency is 29.4912 MHz External clock. If you are using our driver, the PLL will be programmed to the default frequency settings when the driver initializes and can be read or re-programmed by IOCTL calls in the base driver.

Routines to use these calls to read and program the PLL are included in the UserApp code provided in the engineering kit for the board. If you are writing your own driver, contact Dynamic Engineering and we can send you a file with code excerpts from our driver and test software that cover each step of the process from parsing the .jed file to the low-level bit manipulation of the I²C bus.

In normal operation, ccPMC-HOTLink-Kaon1 receives data requests from the TTL I/O line and sends HOTLink data to the target system. This process is repeated about once every 446 microseconds. With the relevant enables and configuration options set; KAON1 will wait to receive TTL data and store it in a 4K by 32-bit FIFO. The HOTLink data to be sent is written to the 32k by 32-bit transmit FIFO. The HOTLink frame format is specified by data written to the 128 by 32-bit format RAM. The RAM need only be loaded once per session, and thereafter the format data will be re-read for each data-frame sent. For loop-back testing the same dual-port RAM is used by the HOTLink receiver to verify the data-frame formatting.

Address Map

Register Name	Offset	Description
HLNK_BASE_CNTRL	0x0000	// Base Control register
HLNK_BASE_USER_INFO	0x0004	// Base User Info read port
HLNK_BASE_STATUS	0x0008	// Base Status read port
HLNK_BASE_PLL_DATA	0x000C	// Base PLL data port
HLNK_CHAN_CNTRL_0	0x0020	// Channel 0 Control register
HLNK_CHAN_STATUS_0	0x0024	// Channel 0 Status register
HLNK_CHAN_FIFO_0	0x0028	// Channel 0 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_0	0x002C	// Channel 0 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_0	0x002C	// Channel 0 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_0	0x0030	// Channel 0 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_0	0x0030	// Channel 0 Receive FIFO data count
HLNK_CHAN_MSG_COUNTS_0	0x0034	// Channel 0 Receive FIFO data count
HLNK_CHAN_TX_AMT_0	0x0038	// Channel 0 TX almost empty level
HLNK_CHAN_RX_AFL_0	0x003C	// Channel 0 RX almost full level
HLNK_CHAN_TTL_CNTRL_0	0x0040	// Channel 0 TTL Control register
HLNK_CHAN_TTL_STATUS_0	0x0044	// Channel 0 TTL Status register
HLNK_CHAN_TTL_FIFO_0	0x0048	// Channel 0 TTL FIFO port
HLNK_CHAN_TTL_FIFO_COUNTS_0	0x004C	// Channel 0 TTL FIFO counts
HLNK_CHAN_CNTRL_1	0x0050	// Channel 1 Control register
HLNK_CHAN_STATUS_1	0x0054	// Channel 1 Status register
HLNK_CHAN_FIFO_1	0x0058	// Channel 1 TX/RX FIFOs single word access
HLNK_CHAN_WR_DMA_PNTR_1	0x005C	// Channel 1 Write DMA physical PCI dpr address
HLNK_CHAN_TX_FIFO_COUNT_1	0x005C	// Channel 1 Transmit FIFO data count
HLNK_CHAN_RD_DMA_PNTR_1	0x0060	// Channel 1 Read DMA physical PCI dpr address
HLNK_CHAN_RX_FIFO_COUNT_1	0x0060	// Channel 1 Receive FIFO data count
HLNK_CHAN_MSG_COUNTS_1	0x0064	// Channel 1 Receive FIFO data count
HLNK_CHAN_TX_AMT_1	0x0068	// Channel 1 TX almost empty level
HLNK_CHAN_RX_AFL_1	0x006C	// Channel 1 RX almost full level
HLNK_CHAN_TTL_CNTRL_1	0x0070	// Channel 1 TTL Control register
HLNK_CHAN_TTL_STATUS_1	0x0074	// Channel 1 TTL Status register
HLNK_CHAN_TTL_FIFO_1	0x0078	// Channel 1 TTL FIFO port
HLNK_CHAN_TTL_FIFO_COUNTS_1	0x007C	// Channel 1 TTL FIFO counts
HLNK_CHAN_FORMAT_RAM_0	0x0200-0x03FC	// Channel 0 Message Frame Format Data
HLNK_CHAN_FORMAT_RAM_1	0x0400-0x05FC	// Channel 1 Message Frame Format Data

FIGURE 5 CCPMC-HOTLINK REGISTER OFFSET ADDRESS MAP

Register Definitions

HLNK_BASE_CNTRL

[0x000] Base Control (read/write)

Base Control Register

Data Bit	Description
31-5	Spare
4	Use Alternate PLL ID
3	Check PLL ID
2	Read PLL
1	Reset PLL
0	PLL Enable

FIGURE 6 CCPMC-HOTLINK BASE CONTROL REGISTER

All bits are active high and are reset on system power-up or reset, except PLL enable, which defaults to enabled (high) on power-up or reset.

PLL Enable: When this bit is set to a one, the PLL programmer module, used to program and read the PLL, is enabled. When this bit is zero, the PLL programmer is disabled.

Reset PLL: When this bit is set to a one, the PLL programmer will stop processing, if not stopped already, and return to its initial state. When this bit is zero, the PLL programmer is ready to accept control inputs.

Read PLL: When this bit is set to a one and the PLL programmer is enabled, the programmer will perform a read of the PLL device internal registers. The 40 bytes of data obtained will be written into the PLL read FIFO as ten long-words. When this bit is zero and the PLL programmer is enabled, the programmer will write data into the PLL device or simply check for a response to the selected ID value depending on the Check PLL ID control bit.

Check PLL ID: When this bit is set to a one and the PLL programmer is enabled, the programmer will begin a write operation, but will stop after the device ID has been sent. If the ID was acknowledged successfully, the done status will be set and the error status will be cleared. If the ID was not acknowledged successfully, the done status will be cleared and the error status will be set. When this bit is zero and the PLL programmer is enabled, the PLL programmer will perform a write or read operation depending on the Read PLL control bit.

Use alternate PLL ID: When this bit is set to a one, the device ID sent will be the alternate ID: 0x6A. When this bit is zero, the normal ID: 0x69 will be sent to the PLL device.

HLNK_BASE_USER_INFO

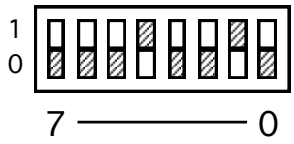
[0x004] Base User Info – (read only)

User Info Port

Data Bit	Description
31-24	FPGA Design Minor Revision
23-16	FPGA Design Revision
15-8	FPGA Design ID
7-0	Switch setting

FIGURE 7 CCPMC-HOTLINK BASE USER INFO PORT

Sw7-0: The user switch is read through this port. The switch bits are read as the lowest byte. Access the read-only port as a long word and mask off the upper 24 bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



FPGA Design ID: The value of the second byte is the design ID, which distinguishes the design from other HOTLink designs. For this design the value is 0x04.

FPGA Design Revision: The value of the third byte of this port is the revision number of the Xilinx design (currently 0x02).

FPGA Design Minor Revision: The value of the second byte of this port is the minor revision number of the Xilinx design (currently 0x03).

HLNK_BASE_STATUS

[0x008] Base Status – (status read / latch clear write)

Base Interrupt Status Register

Data Bit	Description
31-28	Spare
27-20	PCI Core Revision
19	Spare
18	PLL Error
17	PLL Done
16	PLL Ready
15	Spare
14	PLL Read FIFO Data Valid
13	PLL Read FIFO Full
12	PLL Read FIFO Empty
11	Spare
10	PLL Write FIFO Data Valid
9	PLL Write FIFO Full
8	PLL Write FIFO Empty
7	HOTLink Reference Clock DCM Locked
6	PLL Reference Clock DCM Locked
5-2	Spare
1	Channel 1 Interrupt Active
0	Channel 0 Interrupt Active

FIGURE 8 CCPMC-HOTLINK BASE STATUS PORT

Channel Interrupt Active: These two bits are used to report which channel's interrupts are active. When a one is read, it indicates that the corresponding channel has requested an interrupt; when a zero is read, that channel's interrupt is not active.

PLL Reference Clock DCM Locked: When a one is read, it indicates that the PLL reference clock input buffer is frequency locked, when a zero is read the clock input buffer is not in a locked state.

HOTLink Reference Clock DCM Locked: When a one is read, it indicates that the HOTLink reference clock input buffer is frequency locked, when a zero is read the clock input buffer is not in a locked state.

PLL Write/Read FIFO Empty: When a one is read, it indicates that the corresponding FIFO contains no data; when a zero is read, there is at least one word in the FIFO. Although the FIFO is empty, there may still be one valid data word in the pipeline. The FIFO data valid bit indicates whether this is the case.

PLL Write/Read FIFO Full: When a one is read, it indicates that the corresponding FIFO is full; when a zero is read, there is room for at least one word in the FIFO.

PLL Write/Read FIFO Data Valid: When a one is read, there is valid data available; when a zero is read, there is no valid data available.

PLL Ready: When a one is read, the PLL programmer is idle and ready to accept a new command; when a zero is read, the programmer is actively sending data or reading data to/from the PLL device.

PLL Done: When a one is read, the programmer has successfully completed an input or output request; when a zero is read, this is not the case. This bit is latched and must be cleared by writing the PLL done bit back to this register.

PLL Error: When a one is read, an error occurred while processing a read or write request; when a zero is read, no error occurred. This bit is latched and must be cleared by writing the PLL error bit back to this register.

PCI Core Revision: This is the revision that was entered when the core was created, and is the value that is reported to the operating system. Currently this value is 0x00.

HLNK_BASE_PLL_FIFO

[0x00C] PLL Output FIFO Write / PLL Input FIFO Read

PLL Output/Input FIFO Ports	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 9 CCPMC-HOTLINK BASE PLL FIFO PORT

Writes to this port load PLL programming data into the PLL TX FIFO. This data is used to configure the PLL device. Reads from this port return data from the PLL RX FIFO. This data represents the PLL device's internal register state that was read by the PLL programmer. Both FIFOs are 32 words deep and 32 bits wide.

HLNK_CHAN_CNTRL_0-1

[0x020, 0x050] Channel Control (read/write)

Channel Control Register

Data Bit	Description
31-28	Spare
27	HOTLink Initiate Receiver Reframe Sequence
25-26	DMA Word-Count Read Control
24	HOTLink Send Transmit Frame Immediately
22-23	Spare
21	HOTLink Force Receiver Reframe
20	HOTLink Test Mode Enable
19	HOTLink Receiver BIT Enable
18	HOTLink Receiver External Input Select
17	HOTLink Transmitter Load BIT Data Pattern
16	HOTLink Transmitter External Output Enable
15	HOTLink Transmitter BIT Enable
14	HOTLink Transmit TTL Trigger Enable
13	Read DMA Interrupt Enable
12	Write DMA Interrupt Enable
11	HOTLink Receiver Enable
10	RX FIFO Overflow Interrupt Enable
9	RX FIFO Almost Full Interrupt Enable
8	TX FIFO Almost Empty Interrupt Enable
7	Force Interrupt
6	Master Interrupt Enable
5	Read DMA Arbitration Priority Enable
4	Write DMA Arbitration Priority Enable
3	HOTLink Transmitter Enable
2	FIFO Data Loop-Back Test Enable
1	Receive FIFO Reset
0	Transmit FIFO Reset

FIGURE 10 CCPMC-HOTLINK CHANNEL CONTROL REGISTER

All bits are active high and are reset on system power-up or reset. If an external control or status bit is active low, it is inverted from the value in this register.

Transmit/Receive FIFO Reset: When one or both of these bits are set to a one, the corresponding data FIFO and control and status circuitry will be reset. When these bits are zero, normal FIFO operation is enabled. FIFO resets are referenced to the PCI clock; two periods are required for proper reset.

FIFO Data Loop-Back Test Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without sending data to the HOTLink interface. When this bit is zero, normal FIFO operation is enabled.

HOTLink Transmitter Enable: This bit, when set to one, enables the HOTLink transmitter state-machine. The behavior of the transmitter depends on whether there is data in the transmit FIFO, whether a data-frame request has been received from the TTL I/O, as well as the states of the Test Mode Enable and Send Transmit Frame Immediately bit described below. When this bit is zero, the transmitter state-machine is disabled.

Write/Read DMA arbitration priority enable: These two bits, when set to one, enable the DMA arbiter to use the TX almost empty and/or RX almost full status to give priority to a channel that is approaching the limits of its FIFOs. The levels written to the TX almost empty and RX almost full registers are used to determine these status values. When these bits are zero normal round-robin arbitration is used to determine access to the PCI bus for DMA transfers.

Master interrupt enable: When this bit is set to a one all enabled interrupts for the referenced channel (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force interrupt: When this bit is set to a one, a system interrupt will occur provided the channel master interrupt enable is set. This is useful to test interrupt service routines.

TX almost empty interrupt enable: When this bit is set to a one, an interrupt will be generated when the transmit FIFO level is equal or less than the value specified in the HLNK_CHAN_TX_AMT register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register.

RX almost full interrupt enable: When this bit is set to a one, an interrupt will be generated when the receive FIFO level is equal or greater to the value specified in the HLNK_CHAN_RX_AFL register, provided the channel master interrupt enable is asserted. When this bit is zero, an interrupt will not be generated, but the status can still be read from the channel status register.

RX FIFO Overflow Interrupt Enable: When this bit is set to a one, an interrupt will be generated when an attempt is made to write to a full receive FIFO, provided the channel master interrupt enabled is asserted. When a zero is written to this bit, an interrupt will not be generated when an overflow condition occurs, but the latched status can still be read from the channel status register.

HOTLink Receiver Enable: This bit, when set to one, enables the HOTLink receiver state-machine. The HOTLink receiver stores only data bytes. Four bytes are loaded into a 32-bit long-word starting with the least significant byte and are written to the receive FIFO. If a 32-bit word is not completed when the receiver is disabled, the remaining unfilled byte positions will be set to zero and the word will be written to the FIFO. When this bit is zero, the receiver state-machine is disabled.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA write and read completion for the referenced channel. These two interrupts are not disabled by the master interrupt enable.

HOTLink Transmit TTL Trigger Enable: This bit, when set to one, enables transmitter triggered operation. In this mode the transmitter will wait for a trigger from the TTL receiver before sending a data-frame. When this bit is zero, the transmit state-machine will only send data if the Send Transmit Frame Immediately control bit is set. In either mode, when the frame completes, the enable is cleared and the transmitter will wait for another trigger event to send another frame.

HOTLink Transmitter BIT Enable: This bit, when set to one, enables the HOTLink transmitter Built-In-Test mode. When this mode is active, and the Load BIT Data Pattern control bit is asserted, the transmitter sends a repeating test pattern. When this bit is zero, Built-In-Test mode is disabled.

HOTLink Transmitter External Output Enable: This bit, when set to one, enables the external output 'A' of the HOTLink transmitter. When this bit is zero, only the internal output 'C', which is always on, is enabled.

HOTLink Transmitter Load BIT Data Pattern: When the Built-In-Test mode is enabled, setting this bit to a one starts the test sequence. This bit is zero in normal operation.

HOTLink Receiver External Input Select: This bit, when set to one, selects input 'A' on the HOTLink receiver. This input is driven by the external input port. When this bit is zero, input 'B' is selected. This input is driven by the internal signal coming from the channel's HOTLink transmitter output 'C'.

HOTLink Receiver BIT Enable: This bit, when set to one, enables the HOTLink receiver Built-In-Test mode. When this mode is active, and the transmitter is enabled to send the BIT data pattern, the receiver will automatically lock onto this pattern to verify the performance of the link. When this bit is zero, Built-In-Test mode is disabled.

HOTLink Test Mode Enable: This bit enables HOTLink test-mode operation. In test-mode the transmit state-machine, if enabled, will send a 3-byte start sequence, read the transmit FIFO and send data bytes until the transmit data is exhausted. At this point a single stop byte will be sent. The receiver detects the start sequence and stores the subsequent data-bytes into the receive FIFO. When this bit is zero, normal operational mode is enabled. In this mode the transmit state-machine, if enabled, will read the format RAM and the transmit data FIFO and then send format and data bytes in the order specified by the format data until a NULL character is read from the format RAM. The receiver verifies the format bytes, but stores only the data-bytes.

HOTLink Force Receiver Reframe: When this bit is set to one, the reframe signal to the HOTLink receiver will stay asserted constantly. If RF remains HIGH for greater than 2048 bytes, the framer converts to double-byte framing, requiring two K28.5 characters aligned on the same byte boundary within 5 bytes in order to reframe. When this bit is a zero, the framer-control module in the FPGA controls the reframe signal.

HOTLink Send Transmit Frame Immediately: When this bit is set to one, the transmit state-machine sends a data-frame immediately provided there is data in the transmit FIFO. When this bit is a zero and HOTLink Transmit TTL Trigger Enable is a one, the state-machine waits for a trigger signal from the TTL receiver before sending a data-frame.

DMA Word-Count Read Control: These two bits control the value returned when this control register is read. If they are “00” then the normal register contents are returned. If “01” the word-count from the last write DMA is returned. If “10” the word-count from the last read DMA is returned. The respective DMA word-counter is cleared when a new DMA is started. These word-counters are used to get information about DMA’s that failed to complete for some reason.

HOTLink Initiate Receiver Reframe Sequence: When this bit is set to one, a reframe sequence is manually initiated by the framer-control module in the FPGA. When this bit is a zero, the framer-control module waits until it detects at least sixteen symbol violations in a 64-byte period before initiating a reframe sequence.

HLNK_CHAN_STATUS_0-1

[0x024, 0x054] Channel Status (status read/latch clear write)

Channel Status Register

Data Bit	Description
31	Channel Interrupt Active
30	User Interrupt Active
29	Running Disparity Error (latched)
28	Undefined Character Error (latched)
27	Receiver Synched
26	Receiver Active
25	Receiver Done (latched)
24	Transmitter Done (latched)
23	Receive Message Count Error (latched)
22	Receive Framing Error (latched)
21	Transmit Message Count Error (latched)
20	Transmit Underrun (latched)
19	Transmit Data Read (latched)
18	Receive Data Ready (latched)
17	Read DMA Ready (Idle)
16	Write DMA Ready (Idle)
15	Read DMA Error (latched)
14	Write DMA Error (latched)
13	Read DMA Complete (latched)
12	Write DMA Complete (latched)
11	Receive Symbol Error (latched)
10	Receive FIFO Overflow Interrupt Active
9	Receive FIFO Almost Full Interrupt Active
8	Transmit FIFO Almost Empty Interrupt Active
7	Receive Data Valid
6	Receive FIFO Full
5	Receive FIFO Almost Full
4	Receive FIFO Empty
3	Transmit Data Valid
2	Transmit FIFO Full
1	Transmit FIFO Almost Empty
0	Transmit FIFO Empty

FIGURE 11 CCPMC-HOTLINK CHANNEL STATUS REGISTER

Transmit / Receive FIFO Empty: When one is read from one of these bits, the corresponding data FIFO for the specified channel contains no data; when a zero is read, there is at least one data-word in the FIFO.

Transmit / Receive FIFO Almost Empty / Full: When one is read from one of these bits, the number of data-words in the corresponding data FIFO for the specified channel is less than / greater than or equal to the value in the HLNK_CHAN_TX_AMT / HLNK_CHAN_RX_AFL register for that channel; when a zero is read, the level is more / less than that value.

Transmit / Receive FIFO Full: When one is read from one of these bits, the corresponding data FIFO for the specified channel is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Transmit Data Valid: When a one is read, there is at least one valid transmit data word left. This bit can be set even if the transmit FIFO is empty, because there is a one-word pipeline after the FIFO output to feed the transmit I/O or FIFO bypass path. When this bit is a zero, it indicates that there is no more valid transmit data.

Receive Data Valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO status reports empty, because there is a four-word pipeline after the FIFO output to facilitate a PCI read DMA. When this bit is a zero, it indicates that there is no more valid receive data.

Transmit FIFO Almost Empty Interrupt Active: When a one is read, it indicates that the transmit FIFO data count has become less than or equal to the value in the HLNK_CHAN_TX_AMT register. A zero indicates that the FIFO has not become almost empty. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive FIFO Almost Full Interrupt Active: When one, it indicates that the receive FIFO data count has become greater than or equal to the value in the HLNK_CHAN_RX_AFL register. A zero indicates that the FIFO has not become almost full. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive FIFO Overflow Interrupt Active: When a one is read, it indicates that an attempt has been made to write data to a full receive data FIFO. A zero indicates that no overflow condition has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Symbol Error: This is a latched version of the RVS (Received Violation Symbol) signal from the channel's HOTLink receiver. This bit is intended to be used for Built-In-Test operation as it indicates an error during the test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Write/Read DMA Complete: When one, it indicates that the corresponding DMA has completed. These bits are latched and must be cleared by writing the same bit back to this channel status port. A zero indicates that the corresponding DMA has not transitioned from running to completed since the bit was last cleared.

Write/Read DMA Error: When one, it indicates that an error has occurred while the corresponding DMA was in progress. This could be a target or master abort or an incorrect direction bit in one of the DMA descriptors. These bits are latched and must be cleared by writing the same bit back to the channel status port. A zero indicates that no DMA error has occurred.

Write/Read DMA ready (Idle): These two bits report the DMA state-machine status. If a one is read, the corresponding DMA state-machine is idle and available to start a transfer. If a zero is read, the corresponding DMA state-machine is already processing a data transfer.

Receive Data Ready: This is a latched version of the ready signal from the channel's HOTLink receiver. This bit is intended to be used for Built-In-Test operation as the ready signal will pulse once per test loop, so polling this bit will indicate the completion of the receive test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Transmit Data Read: This is a latched version of the data read signal from the channel's HOTLink transmitter. Similar to the ready bit above, this bit is intended to be used for Built-In-Test operation as the data read signal will pulse once per test loop, so polling this bit will indicate the completion of the transmit test sequence. This bit is latched and must be cleared by writing the same bit back to the channel status port.

Transmit Underrun: When one, it indicates that an attempt has been made to read data from an empty transmit data FIFO. A zero indicates that no underrun condition has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Transmit Message Count Error: When one, it indicates that there was a mismatch between the message-frame count stored in the first two bytes of the transmitter format RAM and the number of bytes that were actually sent. A zero indicates that no message count error occurred since this bit was last cleared. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Framing Error: When one, it indicates that there was a framing error in the received data. This could be an incorrect start sequence, a control character received when a data character was expected, a control character that does not match the corresponding character in the format RAM or a data character received when a control character was expected. A zero indicates that no framing error has occurred.

Receive Message Count Error: When one, it indicates that there was a mismatch between the message-frame count stored in the first two bytes of the receiver format RAM and the number of bytes that were actually received. A zero indicates that no message count error occurred since this bit was last cleared. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Transmitter Done: When one, it indicates that a transmitted message-frame has completed since this bit was last cleared. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receiver Done: When one, it indicates that a received message-frame has completed since this bit was last cleared. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receiver Active: When one, it indicates that the receiver has been enabled and started and is in the process of receiving a message. A zero indicates that the receiver is not currently receiving a message.

Receiver Synched: When one, it indicates that the receiver is not out-of-lock and is synchronized to the incoming data stream. A zero indicates that the receiver is not synchronized to the incoming data stream.

Undefined Character Error: When the receiver is not locked and/or has received a violation symbol (RVS), this bit indicates that the receiver has detected an undefined character error. This means that the receiver cannot match the incoming bit pattern to a known data/control character. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Running Disparity Error: When the receiver is not locked and/or has received a violation symbol (RVS), this bit indicates that the receiver has detected a running disparity condition. The disparity can only be plus or minus one. Each character has a disparity value of +/- one or zero. If a received character causes the disparity to exceed +/- one this is an illegal condition. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

User Interrupt Active: When one, it indicates that an enabled user interrupt condition (other than the DMA interrupts) is active for the referenced channel. A zero indicates that no enabled interrupt condition is active.

Channel Interrupt Active: When one, it indicates that the interrupt is active for the referenced channel. A zero indicates that the channel interrupt is not active.

HLNK_CHAN_FIFO_0-1

[0x028, 0x058] TX FIFO Write/RX FIFO Read

RX and TX FIFO Ports	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 12 CCPMC-HOTLINK CHANNEL RX/TX FIFO PORT

These ports are used to make single-word accesses into the channel transmit FIFO and out of the channel receive FIFO.

HLNK_CHAN_WR_DMA_PNTR_0-1

[0x02C, 0x05C] Input DMA Control (write only)

Input DMA Pointer Address Port	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 13 CCPMC-HOTLINK CHANNEL WRITE DMA POINTER PORT

This write-only port is used to initiate a scatter-gather input DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit is set in one of the next pointer values.

HLNK_CHAN_TX_FIFO_COUNT_0-1

[0x02C, 0x05C] TX FIFO Word Count (read only)

TX FIFO Data Count	
Data Bit	**Description**
31-12	Spare
11-0	TX data words stored

FIGURE 14 CCPMC-HOTLINK CHANNEL TX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding transmit FIFO. There is an additional latch that may contain data if enabled, which allows this value to be a maximum of 0x8001.

HLNK_CHAN_RD_DMA_PNTR_0-1

[0x030, 0x060] Output DMA Control (write only)

Output DMA Pointer Address Port	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 15 CCPMC-HOTLINK CHANNEL READ DMA POINTER PORT

This write-only port is used to initiate a scatter-gather output DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit is set in one of the next pointer values.

HLNK_CHAN_RX_FIFO_COUNT_0-1

[0x030, 0x060] RX FIFO Word Count (read only)

RX FIFO Data Count	
Data Bit	**Description**
31-12	Spare
11-0	RX data words stored

FIGURE 16 CCPMC-HOTLINK CHANNEL RX FIFO DATA COUNT PORT

These read-only register ports report the number of 32-bit data words in the corresponding receive FIFO. There are four additional latches in the read DMA pipeline that may contain data, which allows this value to be a maximum of 0x8004.

HLNK_CHAN_MSG_COUNTS_0-1

[0x034, 0x064] Message Counts (read only)

TX and RX Message Counts	
Data Bit	**Description**
31-28	Spare
27-16	Received message byte count
15-12	Spare
11-0	Transmitted message byte count

FIGURE 17 CCPMC-HOTLINK TX/RX MESSAGE COUNT REGISTER

This read only port returns the transmitter and receiver message byte-counts that were seen from the last message processed.

HLNK_CHAN_TX_AMT_0-1

[0x038, 0x068] TX FIFO Almost Empty Level (read/write)

TX FIFO Almost Empty Level Register

Data Bit	Description
31-16	Spare
15-0	TX FIFO almost empty level

FIGURE 18 CCPMC-HOTLINK CHANNEL TX FIFO AMT LEVEL REGISTER

These read/write ports access the transmitter almost-empty level registers for the respective channels. When the number of data words in the transmit data FIFO is equal or less than this value, the almost empty status bit is set and an interrupt may be generated if it is enabled.

HLNK_CHAN_RX_AFL_0-1

[0x03C, 0x06C] RX FIFO Almost Full Level (read/write)

RX FIFO Almost Full Level Register

Data Bit	Description
31-16	Spare
15-0	RX FIFO almost full level

FIGURE 19 CCPMC-HOTLINK CHANNEL RX FIFO AFL LEVEL REGISTER

These read/write ports access the receiver almost-full level registers for the respective channels. When the number of data words in the receive data FIFO is equal or greater than this value, the almost full status bit is set and an interrupt may be generated if it is enabled.

HLNK_CHAN_TTL_CNTRL_0-1

[0x040, 0x070] Channel TTL Control (read/write)

Channel TTL Control Register

Data Bit	Description
31-6	Spare
5	TTL Receiver Done Interrupt Enable
4	TTL Receiver Enable
3	TTL Transmitter Enable
2	TTL FIFO Data Loop-Back Test Enable
1	TTL Receive FIFO Reset
0	TTL Transmit FIFO Reset

FIGURE 20 CCPMC-HOTLINK CHANNEL TTL CONTROL REGISTER

All bits are active high and are reset on system power-up or reset.

TTL Transmit/Receive FIFO Reset: When one or both of these bits are set to a one, the corresponding data FIFO will be reset. When these bits are zero, normal FIFO operation is enabled. FIFO resets are referenced to the PCI clock; two periods are required for proper reset.

TTL FIFO Data Loop-Back Test Enable: When this bit is set to a one, any data written to the TTL transmit FIFO will be immediately transferred to the TTL receive FIFO. This allows for fully testing the data FIFOs without sending data to the TTL interface. When this bit is zero, normal FIFO operation is enabled.

TTL Transmitter/Receiver Enable: When one or both of these bits are set to a one, the corresponding TTL state-machine will be enabled. When a zero is written, the corresponding state-machine will be disabled.

TTL Receiver Done Interrupt Enable: When this bit is set to a one and the master interrupt enable is asserted, an interrupt will be generated when a TTL data-frame has been received. The frame consists of a start-of-frame (2 clock cycles) and 60 bytes of data (960 clock cycles) at which point the receiver done interrupt will be generated. After the data segment is completed and the interrupt has been asserted, 1050 zeros are received (2110 clock cycles) for a total of 3072 clock cycles. This process repeats until the interface is disabled. When a zero is written, the TTL receiver interrupt will not be generated although the receive frame done status bit will still be latched.

HLNK_CHAN_TTL_STATUS_0-1

[0x044, 0x074] Channel TTL status read/latch clear write

Channel TTL Status Register

Data Bit	Description
31-12	Spare
11	TTL Receiver Start-of-Frame Missing
10	TTL Received Frame Done
9	TTL Receive FIFO Overflow
8	TTL Receiver Bit Error
7	TTL Receive FIFO Data Valid
6	TTL Receive FIFO Full
5	TTL Receive FIFO Almost Full
4	TTL Receive FIFO Empty
3	TTL Transmit FIFO Data Valid
2	TTL Transmit FIFO Full
1	TTL Transmit FIFO Almost Empty
0	TTL Transmit FIFO Empty

FIGURE 21 CCPMC-HOTLINK CHANNEL TTL STATUS REGISTER

TTL Transmit FIFO Empty: When a one is read, TTL transmit data FIFO contains no data; when a zero is read, there is at least one data-word in the FIFO.

TTL Transmit FIFO Almost Empty: When a one is read, the referenced TTL transmit data FIFO word-count is less than or equal to16; when a zero is read, there is at least 17 words of data in the FIFO.

TTL Transmit FIFO Full: When a one is read, the TTL transmit data FIFO is full; when a zero is read, there is room for at least one more data-word in the FIFO.

TTL Transmit FIFO Data Valid: When a one is read, there is at least one valid TTL data word left. This bit can be set even if the TTL FIFO is empty, because there is a one-word pipeline after the FIFO output. When this bit is a zero, it indicates that there is no more valid TTL data.

TTL Receive FIFO Empty: When a one is read, the TTL received data FIFO contains no data; when a zero is read, there is at least one data-word in the FIFO.

TTL Receive FIFO Almost Full: When a one is read, the TTL received data FIFO word-count is greater than or equal to 4080; when a zero is read, there is less than 4080 words of data in the FIFO.

TTL Receive FIFO Full: When a one is read, the TTL received data FIFO is full; when a zero is read, there is room for at least one more data-word in the FIFO.

TTL Receive FIFO Data Valid: When a one is read, there is at least one valid TTL data-word in the receive FIFO. This bit can be set even if the FIFO is empty, because there is a one-word pipeline after the FIFO output. When this bit is a zero, it indicates that the TTL received data FIFO contains no valid data.

TTL Receiver Bit Error: When a one is read, it indicates that an error occurred in the bit decode process. A zero means that no bit decoding error has occurred since this bit was last cleared. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

TTL Receive FIFO Overflow: When a one is read, it indicates that an attempt has been made to write data to a full TTL received data FIFO. A zero indicates that no overflow condition has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

TTL Received Frame Done: When a one is read, it indicates that a received data-frame has completed. A zero means that a received data-frame has not completed since this bit was last cleared. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

TTL Receiver Start-of-Frame Missing: When a one is read, it indicates that the TTL start-of-frame was not seen when it was scheduled to occur. The data-frame is precisely 3072 clocks long and the start-of-frame is expected when this interval expires. When a zero is read, it means that the start-of-frame was not missed since this bit was last cleared. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

HLNK_CHAN_TTL_FIFO_0-1

[0x048, 0x078] TTL FIFO (read/write)

TTL FIFO Port	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 22 CCPMC-HOTLINK CHANNEL TTL FIFO PORT

This port is used to make single-word accesses to/from the channel transmit/receive TTL FIFOs.

After receiving data the first LW read contains 31-16 = First Word, 15-8 = Frame number, 7-0 = x80. Data is loaded 3210 for the byte order there after.

Please note 7-0 was x01 for revisions prior to 2p3.

HLNK_CHAN_TTL_FIFO_COUNTS_0-1

[0x04C, 0x07C] TTL FIFO (read only)

TTL FIFO Word Counts	
Data Bit	**Description**
31-29	Spare
28-16	TTL Receive FIFO Word Count
15-13	Spare
12-0	TTL Transmit FIFO Word Count

FIGURE 23 CCPMC-HOTLINK CHANNEL TTL FIFO WORD COUNTS

This read-only register port reports the number of 32-bit data words in the transmit and receive TTL FIFO. There is one additional latch in each of the data pipelines that may contain data, which allows the count values to be a maximum of 0x1001 words.

Loop-back

The “UserAp” reference software includes external loop-back tests. Both same port and across port SW tests are included. The pinouts are below. In addition, memory, PLL programming and other utilities are included.

The I/O signals are only available on PN4. A PMC carrier is needed to access the PN4 signals. Below are the pinouts for any Dynamic Engineering “X1” type carrier / adapter. For example, PCIeBPMCX1 [adapts PMC to PCIe] and PCIBPMCX1 [adapts PMC to PCI]. In addition, the pinouts are compatible with PMC-UNIV-TEST. A 68-pin SCSI II connector on the carrier connects to the I/O signals from PN4. If you use a different carrier, these pins may change.

	Same Channel Loopback			
SIGNAL	+	-	+	-
HSS 0->0	57	23	35	1
HSS 1->1	24	58	36	2
TTL 0->0	43		59	
TTL 1->1	45		26	

	Cross Channel Loopback			
SIGNAL	+	-	+	-
HSS 0->1	57	23	36	2
HSS 1->0	24	58	35	1
TTL 0->1	43		26	
TTL 1->0	45		59	

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on ccPMC-HOTLink. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 24 CCPMC-HOTLINK PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module Pn2 Interface on ccPMC-HOTLink. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 25 CCPMC-HOTLINK PN2 INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for ccPMC-HOTLink-KAON1 Module Pn4. Also, see the User Manual for your carrier board for information on interfacing with Pn4.

HSSIN_0+	HSSIN_1+	1	2
HSSIN_0-	HSSIN_1-	3	4
		5	6
		7	8
		9	10
		11	12
		13	14
		15	16
TTLOUT_0		17	18
		19	20
TTLOUT_1		21	22
		23	24
		25	26
		27	28
		29	30
		31	32
		33	34
		35	36
		37	38
		39	40
		41	42
		43	44
HSSOUT_0+	HSSOUT_1-	45	46
HSSOUT_0-	HSSOUT_1+	47	48
TTLIN_0		49	50
	TTLIN_1	51	52
		53	54
		55	56
		57	58
		59	60
		61	62
		63	64

FIGURE 26 CCPMC-HOTLINK-KAON1 PN4 INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling ccPMC-HOTLink. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card, the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. In a windows system the “Device Manager” can be used. In a Linux system “lspci” can be useful to gain system information about the installed hardware.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. ccPMC-HOTLink is constructed out of 0.062-inch thick High Temperature ROHS compliant FR4 material.

Through-hole and surface-mount components are used. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration please contact Dynamic Engineering to glue the larger components after final QA.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The ccPMC-HOTLink design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. The board is conduction-cooled, therefore low thermal impedance to the carrier cooling rails and surfaces is imperative. If using forced air, with the one-degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the repair charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 Dubois Street, Suite C
Santa Cruz, CA 95060
831-457-8891
support@dyneng.com

Specifications

Host Interface (PMC):	PMC(PCI Mezzanine Card)
Serial Interfaces:	Two HOTLink inputs and two HOTLink outputs [PECL] Two TTL inputs and two TTL outputs [AC coupled]
TX Bit-rates generated:	167.77216 Mbytes/sec for the HOTLink I/O, 6.88128 Mbits/sec for the TTL I/O Frequencies can be varied by reprogramming the PLL
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory map)
Wait States:	One for all addresses
Interrupt:	Each channel has an interrupt for TX almost empty, RX almost full, and RX FIFO overflow. Read and write DMA interrupts are also implemented for each channel.
DMA:	Independent input and output Bus-Master Scatter/Gather DMA Support implemented for each channel
Onboard Options:	All Options are Software Programmable
Interface Options:	All HOTLink and TTL I/O lines are available on Pn4 only
Dimensions:	Standard Single PMC Module
Construction:	FR4 Multi-Layer Printed Circuit, Surface-Mount Components
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	5V, 3.3V

Order Information

ccPMC-HOTLink-KAON1	https://www.dyneng.com/ccPmcHOTLink.html Standard version with two 32K x 32-bit FIFOs [HOTLink], and two 4K x 32-bit FIFOs[TTL] per channel. Two channels, I/O on Pn4. Industrial Temperature standard. 32/33 PCI interface.
-ROHS	Switch to ROHS compatible solder.
PMC-UNIV-TEST	https://www.dyneng.com/PMC-UNIV-TEST.html small form extender to mount PMC vertically oriented in PCI slot. Test Points on PCI signals. Jn1, Jn2, Jn4 supported. Jn4 routed to SCSI connector [differential, 100 ohms]. Option for engineering model with full pass through [installed between carrier and PMC to expose PCI bus]
SCSI cable	3Ft, 6Ft, 9Ft stocked. Latch block or thumbscrew. Compatible with PMC-UNIV-TEST and most Dynamic Engineering PMC & XMC carriers. https://www.dyneng.com/HDEcabl68.html

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