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User Manual

PMC BiSerial-II NG1

Bi-directional Serial Data Interface PMC Module

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PMC BiSerial-II NG1
Bi-Directional Serial Data Interface PMC Module

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The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with PMC Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Product Description

The PMC BiSerial-II NG1 is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC BiSerial-II is capable of providing multiple serial protocols. The NG1 protocol implemented provides two full-duplex RS-422 UART interfaces with error detection, two half-duplex RS-485 custom “index” interfaces, external clock input, two clock outputs, and various discrete signal inputs and outputs, all using RS-485 transceivers.

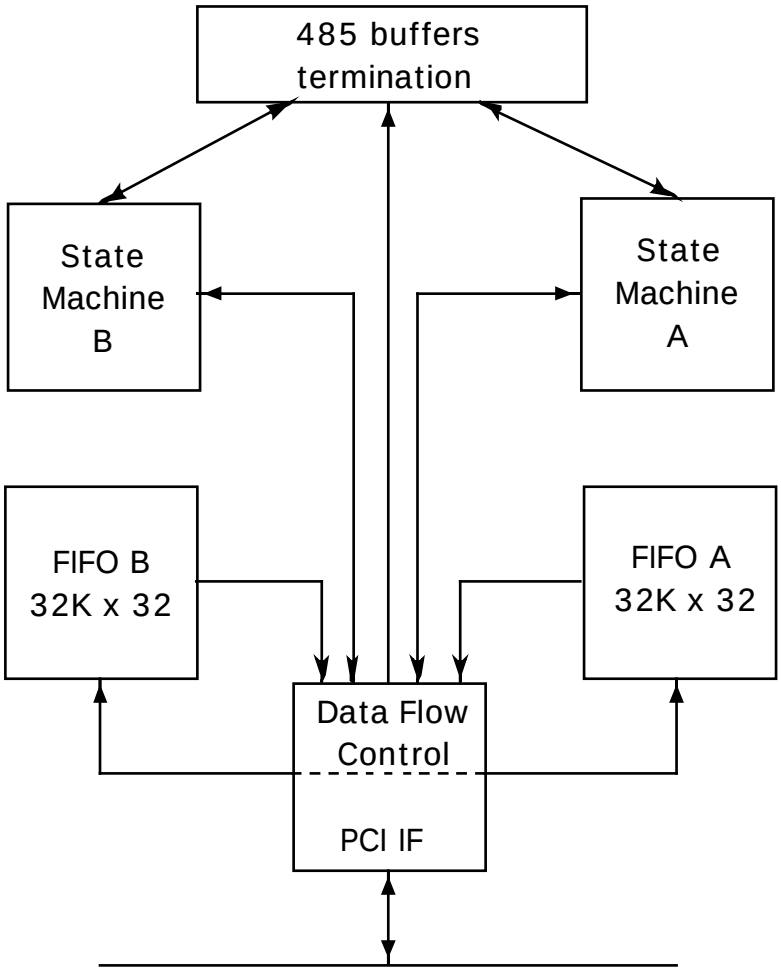

FIGURE 1 PMC BISERIAL-II BLOCK DIAGRAM

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a "standard" special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

The transmit data rate is derived from the 31.25 MHz on-board oscillator or external reference clock. The 31.25 MHz clock is divided by 2, 3, 4, 5, 6, 7, or 8 to generate the external clock outputs as well as the Tx clock for the UART and index interfaces.

The receive side of these interfaces uses a doubled (62.5 MHz) clock to sample the input data stream. The receiver uses the clock divisor to determine how many clock periods constitute a received bit period.

The FIFOs always operate at the PCI clock frequency of 33 MHz to simplify testing and operational functions.

Thirty-two differential I/O are provided for the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 100Ω (82Ω resistor plus internal switch resistance). The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. Optional pullup/pulldown resistor packs can also be installed to provide a logic '1' on undriven lines. The terminations and transceivers are programmable through the Xilinx device to provide the proper mix of outputs and inputs and terminations needed for a specific protocol implementation.

All configuration registers support read and write operations for maximum software convenience, and all addresses are long word aligned.

The PMC BiSerial-II conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

The PMC BiSerial-II uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard

connectors [height] to mate with the PMC BiSerial-II, please let us know. We may be able to do a special build with a different height connector to compensate.

The UART channels are each supported by a 32K by 32-bit FIFO. The FIFOs support long word reads and writes with a full 32-bit loop-back path for FIFO testing. Data is latched and the bus immediately released on a write-cycle. As soon as data is present in the FIFO it is pre-read to be immediately available for a read cycle. This allows minimal delay on the PCI write or read to/from the FIFO, as well as immediate access for the Tx and Rx state machines.

A 2048 by 8-bit internal FIFO is also provided for each UART channel to store response data. This FIFO can only be written to by the Rx state machine when receiving an acknowledge packet after a read or write packet has been sent. The response data is read over the PCI bus by the user software.

The index channels send a 9-bit data word when it is loaded into their data register, if enabled to do so. An immediate response of 9 or 12 bits is expected, which is stored in an internal register. The data available flag is set, which can be enabled to cause an interrupt, and the received data can be read over the PCI bus. Each channel has a separate direction output, which indicates whether the channel is currently functioning in transmit or receive mode.

The index channels can also send data from one or both of two pre-programmed data registers every 10 µsec. If both registers are enabled the data word alternates between the two values. A12-bit loop count is provided to determine the number of words sent. If the loop count is zero the process will continue indefinitely.

An external clock input is available to receive an external 31.25 MHz clock reference. This input can also be used to receive a 1x data clock at the desired transfer frequency.

Two separately enabled clock outputs send the programmed transmit clock off the board for use by external circuitry.

There are five other bi-directional discrete I/O lines, two Error signals (Error1 and Error2), an Alive signal, a Clock Select signal, and a Spare signal. The direction and value of these signals is programmable with configuration register bits, when set to be an output, and read as a status bit, when set to be an input.

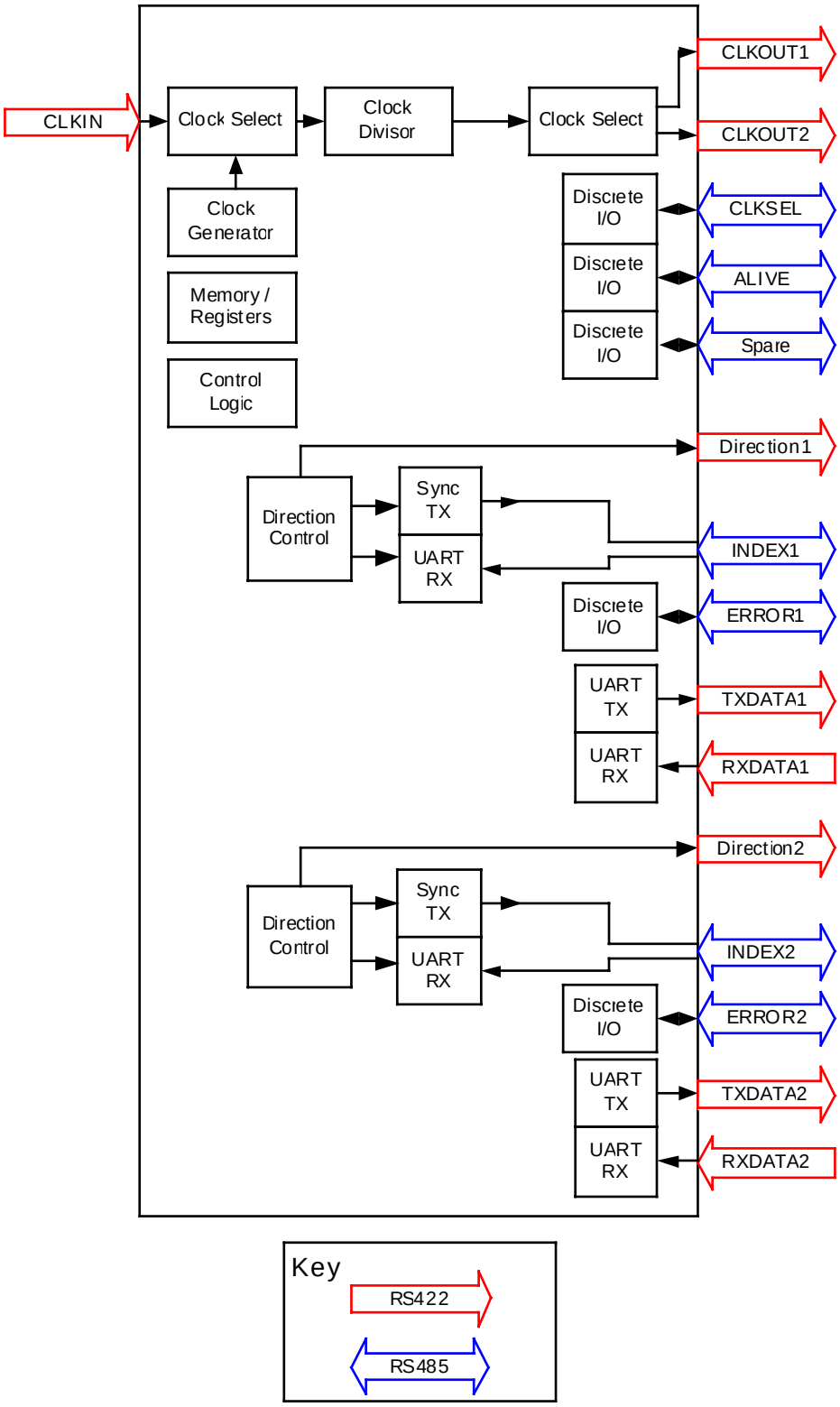

FIGURE 2 NG1 FUNCTIONAL BLOCK DIAGRAM

Various interrupts are supported by the PMC BiSerial-II NG1. An interrupt can be configured to occur when either FIFO becomes almost full or almost empty, when either response FIFO goes above ¾ full or below ¼ full, when index data is available or an index framing error is detected, or when either UART channel or either index channel times-out.

Theory of Operation

The PMC BiSerial-II NG1 features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the BiSerial-II design. Only the transceivers, switches, and external FIFOs are external to the Xilinx device.

The PMC BiSerial-II is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. In standard configuration, the PMC BiSerial-II is a Type 1 mechanical with no components on the back of the board and one slot wide, with 10 mm inter-board height. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design.

The PCI interface to the host CPU is controlled by a logic block within the Xilinx. The BiSerial-II design requires one wait state for read or write cycles to any address. The PMC BiSerial-II is capable of supporting 40 MBytes per second into and out of the FIFOs. The wait states refer to the number of clocks after the PCI core decode before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate with data state into the TRDY signal.

The BiSerial-II can support many protocols. The PMC BiSerial-II NG1 uses seven RS-485 bi-directional I/O, six RS-422 outputs, and three RS-422 inputs to implement a variety of interfaces.

There is an onboard 31.25 MHz oscillator used to derive clock rates used by the serial interfaces. There is also an external clock input that receives either a 31.25 MHz reference or a 1x clock at the desired transfer frequency. A three-bit field in the base configuration register determines the operational frequency for all interfaces on the board. Two external clock outputs can be individually enabled to send this clock off the board.

The two UART interfaces each use an RS-422 input and output. This interface sends packets of six to eight bytes and receives an acknowledge of five bytes for a read packet, or two bytes for a write packet or a read packet that contains errors. The last byte of the transmitted packets and the five-byte response is a cyclic redundancy code (CRC) that is used to verify data integrity. Parity, framing,

and packet length errors are also detected and reported in the acknowledge packets.

Each UART channel on the PMC BiSerial-II NG1 can be configured to be a controller (initiates transfers), or a terminal (responds to transfers). If a controller does not receive a response to a packet within 1 msec., a time-out condition occurs, a status bit is set and, if configured, an interrupt occurs.

The two Index interfaces each use a single bi-directional RS-485 I/O line. This interface sends a nine-bit word and receives an immediate nine or 12-bit response. The first nine bits of the response are an echo of the transmit word. The last three optional bits are status bits that have been pre-written into a register. See the diagram below.

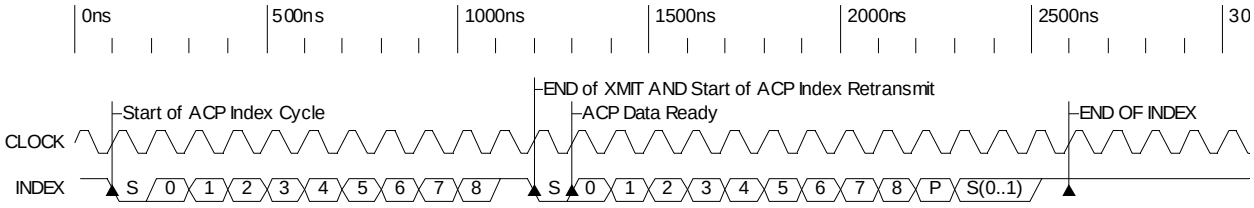

FIGURE 3 INDEX INTERFACE TIMING DIAGRAM

Each Index channel can be configured to transmit first and wait for a response, or to receive a transmitted word and respond appropriately. If a channel that has been programmed to transmit first does not receive a response within one clock plus a programmable value (0 to 240 in 16 nsec. increments) a time-out condition occurs, a status bit is set and, an interrupt may occur if enabled. Each Index interface has an additional RS-422 direction output associated with it that indicates whether the interface is currently operating as an output or an input.

The receive side of both UART and Index interfaces uses a doubled (62.5 MHz) clock to sample the input data stream until a low start bit is detected. The data value is sampled at the middle of each bit slot according to the clock divisor selected. If a transition is detected one 62.5 MHz clock earlier or later than the expected transition from one bit to the next, the count will re-synchronize to this new transition. This allows the receiver to tolerate greater variation in the received data rate.

In addition to the IO signals already discussed, there are five static bi-directional signals. These include two Error signals controlled from the Index configuration registers, an Alive signal, a Clock Select signal, and a Spare signal all controlled from the base configuration register. When these signals are configured as inputs, there value can be read in the StatO status register. When they are configured as outputs, the output value is defined by a register bit with the exception of the Alive signal, which has multiple configurations.

The Alive output can be configured to send a positive pulse of either one msec or ten msec. The pulse width and the signal to send the pulse are set by register bits. The send bit clears itself at the end or the Alive pulse and is ready to send another pulse by resetting the bit. The Alive signal can also be configured to detect the presence of an external clock if it has been selected as the clock reference. If the clock is missing the Alive signal will go high until a clock is detected.

When Alive is configured as an input, it will set a latch when a one is detected. This latch bit will remain set until the StatO status register is read, at which time it will be cleared until the input once more is high. When Alive is set to detect the external clock, it will also set this latch bit when the clock is not detected.

Address Map

REGISTER	OFFSET	FUNCTION	TYPE
BIS2_BASE	EQU $00	Base control register	read/write
BIS2_INTEN	EQU $04	Interrupt enables	read/write
BIS2_UART1	EQU $08	UART 1 control	read/write
BIS2_UART2	EQU $0C	UART 2 control	read/write
BIS2_INDEX1	EQU $10	Index 1 control	read/write
BIS2_INDEX2	EQU $14	Index 2 control	read/write
BIS2_STAT0	EQU $18	Status register 0	read
BIS2_SW_IN	EQU $1C	User switch port	read
BIS2_INDEX1_DATA	EQU $20	Index 1 Tx/Rx data	read/write
BIS2_INDEX1_TX1	EQU $24	Index 1 Transmit data1	read/write
BIS2_INDEX1_TX2	EQU $28	Index 1 Transmit data2	read/write
BIS2_INDEX2_DATA	EQU $2C	Index 2 Tx/Rx data	read/write
BIS2_INDEX2_TX1	EQU $30	Index 2 Transmit data1	read/write
BIS2_INDEX2_TX2	EQU $34	Index 2 Transmit data2	read/write
BIS2_UART1_DATA	EQU $38	FIFO A data port	read/write
BIS2_UART2_DATA	EQU $3C	FIFO B data port	read/write
BIS2_TERM	EQU $40	Termination control	read/write
BIS2_STAT1	EQU $44	Status register 1	read/write
BIS2_DATA_READ1	EQU $48	UART 1 read request data	read/write
BIS2_DATA_READ2	EQU $4C	UART 2 read request data	read/write
BIS2_RESP1_DATA	EQU $50	UART 1 response FIFO	read
BIS2_RESP 2_DATA	EQU $54	UART 2 response FIFO	read

FIGURE 4 PMC BISERIAL-II INTERNAL ADDRESS MAP

The address map provided is for the local decoding performed within the PMC BiSerial-II NG1. The addresses are all offsets from a base address, which is assigned by the system when the PCI bus is configured.

The VendorId = Ox10EE. The CardId = Ox0013. Current revision = E

Programming

Programming the PMC BiSerial-II NG1 requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PMC BiSerial-II NG1 "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

In order to transfer data, first enable the clock, select the clock source, and specify the divisor in the base configuration register. The same clock will be used for both of the Index and UART data interfaces.

The Index interface has two modes of sending data. In the auto mode, data is pre-loaded into one or both of the Tx data registers and the appropriate register(s) enabled. The number of iterations desired is entered in the loop count field or zero to loop indefinitely and auto mode enabled. Data words will be sent every 10 µsec. alternating between the data registers, if both are enabled, until the loop count is satisfied.

In the normal mode, a data word is written into the index data register and it is automatically shifted out with start and stop bits added. When data is received, the index data available flag will be set in the Stat1 status register, and the data can be read from the same address.

To send data over the UART channel, the channel must be configured as a controller and the data must first be loaded into one of the 32k x 32-bit FIFOs through the UART1 or 2 data port. Two 32-bit words are needed for a packet, which may be six, seven, or eight bytes, depending on the address field size. The last byte of the packet is a CRC error check that is calculated in software for the transmitted data, but is automatically verified in hardware on the receive side. The CRC for the five-byte read response is also calculated by the hardware. After one or more packets are loaded into a FIFO, the packets can be sent out one at a time or all at once. After a packet has been sent, the controller waits up to one millisecond for a response before reporting a time-out error. The response data is stored in a separate 2048 x 8-bit FIFO that is internal to the Xilinx FPGA.

If the channel is configured as a terminal it waits until it receives a packet, checks for errors and generates a response. The received packet is stored in the external FIFO and the internal response FIFO is not used.

Before data is transferred, the interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the programmable almost full or empty interrupts, the response FIFO ¾ or ¼ full interrupts, the Index data available interrupts, or various error conditions.

Refer to the Theory of Operation section above and the Interrupts section below for more information regarding the exact sequencing and interrupt definitions.

Register Definitions

BIS2_BASE

[$00] BiSerial-II Base Control Register Port read/write

CONTROL BASE

DATA BIT	DESCRIPTION
31-24	spare
23	Spare out
22	Spare direction
21	Clock select out
20	Clock select direction
19	Alive pulse width
18	Alive clock detect
17	Alive send pulse
16	Alive direction
15	spare
14	External clock2 output enable
13	External clock1 output enable
12	Clock enable
11	External clock select
10-8	Clock divisor (clock = 31.25/n+1)
7	FIFO B Loop Test
6	FIFO A Loop Test
5	1 = Load B almost levels, 0 = Data accesses
4	1 = FIFO B enabled, 0 = FIFO B reset
3	1 = Load A almost levels, 0 = Data accesses
2	1 = User Switch Enabled, 0 = Normal
1	Spare
0	1 = FIFO A enabled, 0 = FIFO A reset

FIGURE 5 PMC BISERIAL-II BASE CONTROL REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

Spare out is the data value sent on this I/O line when it is configured as an output.

Spare direction determines the direction of the spare I/O line. If this value is one, it is configured as an output; if spare direction is a zero it is an input.

Clock select out is the data value sent on this I/O line when it is configured as an output.

Clock select direction determines the direction of the clock select I/O line. If this value is one, it is configured as an output; if clock select direction is a zero it is an input.

Alive pulse width determines the width of the alive pulse when configured to send a pulse. When this bit is a one, the pulse width will be 10 msec; when zero, the pulse width will be 1 msec.

Alive clock detect when set to a one, configures the alive signal to go high if the external clock is selected and the external clock is missing; when zero the alive signal will only respond to the send pulse bit.

Alive send pulse when set to a one, sends a pulse on the alive I/O line, provided it is configured as an output. This bit will self-clear at the end of the pulse so it is not necessary to write a zero.

Alive direction determines the direction of the alive I/O line. If this value is one, it is configured as an output; if alive direction is a zero it is an input.

External clock2 output enable when set to a one enables the clock onto the external clock2 I/O line.

External clock1 output enable when set to a one enables the clock onto the external clock1 I/O line.

Clock enable when set to a one enables the operational clock to the various state machines and external clock outputs. When this bit is zero, the UART and Index interfaces will not function and the external clock outputs will be disabled. However, the static signals will still operate as before.

External clock select when set to a one uses the external clock input as the clock reference to derive the operational clocks. When this bit is a zero, the onboard oscillator is used as the clock reference.

Clock divisor is a three-bit field that determines the operational clock frequency. The operational clock equals the reference clock divided by this value plus one e.g. if clock divisor = 2, the frequency = 31.25/3 = 10.417. If this field is zero and the external clock reference is selected, the clock generator expects a one times clock on the external clock input. This clock will be used as an input to a digital phase locked loop that uses the onboard oscillator as a reference to generate a 62.5 MHz clock and clock divisor values to be used by the UART and Index Tx and Rx interfaces.

FIFO A, B Loop Test when set to a one allows both reading and writing of the FIFO from the PCI bus. This is used to test the FIFOs.

Load A Load B controls the loading and reading of the almost full/empty flag levels. When this bit is a one, FIFO read/write accesses are redirected to the level registers in sequential order Almost Empty, Almost Full, Almost Empty etc. When zero, normal data accesses are enabled. The level of this signal when the respective FIFO is reset determines the default levels at which the almost full/empty signals operate and the method used to reprogram these levels. If Load is high when reset is asserted, parallel programming is enabled and the default offset is 63 words, if low, serial programming is enabled and the default offset is 7 words, serial programming of the almost full/empty flags is not supported by this hardware.

Enable A Enable B enables and resets the FIFO. When this bit goes low the FIFO is reset and when it is one the FIFO is enabled. A reset sequence should be performed after power up before FIFO writes can take place.

User switch enable gates the user dipswitch value onto the lower eight data lines for FIFO A when this bit is a one. A zero value enables normal FIFO access.

BIS2_INTEN

[$04] BiSerial-II Interrupt Enable Register Port read/write

CONTROL INTERRUPT ENABLE	
DATA BIT	**DESCRIPTION**
31-18	Spare
17	Master Interrupt Enable
16	Force Interrupt
15	Response FIFO 2 ¾ full int enable
14	Response FIFO 2 ¼ full int enable
13	Response FIFO 1 ¾ full int enable
12	Response FIFO 1 ¼ full int enable
11	FIFO B almost full int enable
10	FIFO B almost empty int enable
9	FIFO A almost full int enable
8	FIFO A almost empty int enable
7	UART2 time-out error int enable
6	Index2 time-out error int enable
5	Index2 framing error int enable
4	Index2 data available int enable
3	UART1 time-out error int enable
2	Index1 time-out error int enable
1	Index1 framing error int enable
0	Index1 data available int enable

FIGURE 6 PMC BISERIAL-II INTERRUPT ENABLE REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

Master Interrupt Enable must be set to a one in order to cause a system interrupt when an enabled interrupt condition occurs. When this bit is zero, all interrupts are disabled.

Force Interrupt causes a system interrupt when set to a one if Master Interrupt Enable is asserted. This bit is used to test interrupt processing.

Response FIFO 2 ¾ full int enable when set to a one, enables the ¾ full interrupt for response FIFO 1. This interrupt occurs when the FIFO level changes from below ¾ full to below ¾ full or above.

Response FIFO 2 ¼ full int enable when set to a one, enables the ¼ full interrupt for response FIFO 1. This interrupt occurs when the FIFO level changes from ¼ full or above to below ¼ full.

Response FIFO 1 ¾ full int enable when set to a one, enables the ¾ full interrupt for response FIFO 1. This interrupt occurs when the FIFO level changes from below ¾ full to below ¾ full or above.

Response FIFO 1 ¼ full int enable when set to a one, enables the ¼ full interrupt for response FIFO 1. This interrupt occurs when the FIFO level changes from ¼ full or above to below ¼ full.

FIFO B almost full int enable when set to a one, enables the FIFO B almost full interrupt. This occurs when FIFO B becomes almost full as defined by the FIFO almost full flag register.

FIFO B almost empty int enable when set to a one, enables the FIFO B almost empty interrupt. This occurs when FIFO B becomes almost empty as defined by the FIFO almost empty flag register.

FIFO A almost full int enable when set to a one, enables the FIFO A almost full interrupt. This occurs when FIFO A becomes almost full as defined by the FIFO almost full flag register.

FIFO A almost empty int enable when set to a one, enables the FIFO A almost empty interrupt. This occurs when FIFO A becomes almost empty as defined by the FIFO almost empty flag register.

UART 2 time-out error int enable when set to a one, enables the UART 2 time-out error interrupt. This occurs when a response is not received within one millisecond after a packet is sent.

Index 2 time-out error int enable when set to a one, enables the Index 2 time-out error interrupt. This occurs when a response is not received within one clock plus 0 to 240 nsec, as determined by the index time-out field, after a data word is sent.

Index 2 frame error int enable when set to a one, enables the Index 2 framing error detected interrupt. This occurs when the receiver level is not high when the stop bit should be being received.

Index 2 data available int enable when set to a one, enables the Index 2 data available interrupt. This occurs when a data word is received by the Index 2 receiver.

UART 1 time-out error int enable when set to a one, enables the UART 1 time-out error interrupt. This occurs when a response is not received within one millisecond after a packet is sent.

Index 1 time-out error int enable when set to a one, enables the Index 1 time-out error interrupt. This occurs when a response is not received within one clock plus 0 to 240 nsec, as determined by the index time-out field, after a data word is sent.

Index 1 frame error int enable when set to a one, enables the Index 1 framing error detected interrupt. This occurs when the receiver level is not high when the stop bit should be being received.

Index 1 data available int enable when set to a one, enables the Index 1 data available interrupt. This occurs when a data word is received by the Index 1 receiver.

BIS2_UART1,2

[$08, $0C] BiSerial-II UART1,2 Control Register Port read/write

CONTROL UART1,2	
DATA BIT	**DESCRIPTION**
31	CRC error inject
30	Parity error inject
29	Framing error inject
28	Packet length error inject
27-24	LRU 4 ID number
23-20	LRU 3 ID number
19-16	LRU 2 ID number
15-12	LRU 1 ID number
11-8	LRU 0 ID number
7	Send 1 packet
6	Send packets
5	Dual acknowledge enable
4	2 stop bits enable
3	Parity odd
2	Parity enable
1	Controller enable
0	UART enable

FIGURE 7 PMC BISERIAL-II UART1,2 CONTROL REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

CRC error inject when set to a one causes the acknowledge response to register a CRC error regardless of whether this actually occurred. When zero, the state of the CRC error bit is solely determined by the comparison of CRC calculated and CRC received.

Parity error inject when set to a one causes the acknowledge response to register a parity error regardless of whether this actually occurred. When zero, the state of the parity error bit is solely determined by the comparison of the parity calculated and the parity received.

Framing error inject when set to a one causes the acknowledge response to register a framing error regardless of whether this actually occurred. When zero, the state of the framing error bit is solely determined by the actual detection of a framing error in the received packet.

Packet length error inject when set to a one causes the acknowledge response to register a packet length error regardless of whether this actually occurred. When zero, the state of the packet length error bit is solely determined by the comparison of the number of packets received and the packet length field in the received packet.

LRU 0..4 ID numbers determines the LRU ID numbers, which the UART recognizes as valid. If the LRU field in a received packet fails to match any of these values, the ID ERR bit in the acknowledge packet will be set, otherwise the bit will be cleared. If only one ID is desired to be valid, enter the same value in all five fields.

Send 1 packet when set to a one and at least two data words are present in the FIFO, one packet will be sent. The bit clears automatically, so the bit does not need to be written as a zero after transmission. Each time the bit is written as a one, one packet will be sent.

Send packets when set to a one and at least two data words are present in the FIFO causes packets to be sent until no more data is available. When this bit is a zero, no additional packets will be sent.

Dual acknowledge enable when set to a one causes a UART configured as a controller to expect two acknowledge packets, and a UART configured as a terminal to generate two acknowledge packets. When this bit is a zero only a single acknowledge packet will be generated. If the data packet was a read packet containing no errors, the first response packet of the dual acknowledge will be an acknowledge 1 and the second response packet of the dual acknowledge will be an acknowledge 2, otherwise they will both be acknowledge 1 packets.

2 stop bits enable when set to a one causes to two stop bits to be added to each transmitted byte and two stop bits to be checked for by the receiver. When this bit is a zero, only one stop bit will be generated and expected.

Parity odd when set to a one, causes the parity generator, when enabled, to calculate odd parity to determine the value of transmit parity bit and to verify the received parity bit. When this bit is a zero, even parity is calculated.

Parity enable when set to a one, enables the parity generator to calculate the parity bit to determine the value of transmit parity bit and to verify the received parity bit. When this bit is a zero, the parity bit is always set to zero.

Controller enable when set to a one, configures the UART as a controller. This means that it instigates transmissions and waits for a response. When this bit is a zero, the UART is configured as a terminal. This means it waits to receive a packet and then generates a response.

UART enable when set to a one enables the UART to send and receive data as determined by the other configuration bits. When this bit is a zero, the UART is completely disabled.

BIS2_INDEX1,2

[$10, $14] BiSerial-II Index1,2 Control Register Port read/write

CONTROL INDEX1,2

DATA BIT	DESCRIPTION
31	Invert msb
30-20	Index loop count
19-16	Index time-out
15-12	Index Tx phase
11	Index Tx2 enable
10	Index Tx1 enable
9	Error direction
8	Error output value
7	Index auto-terminate
6-4	Index status response
3	Index auto-transmit enable
2	Index response size
1	Index Tx_Rx
0	Index Enable

FIGURE 8 PMC BISERIAL-II INDEX1,2 CONTROL REGISTER BIT MAP

All bits are active high and are reset on power-up or reset command.

Invert msb, when set to a one, causes the msb of the echoed data value to be inverted from the value received. When this bit is a zero, the echoed data value is the same as the value received.

Index loop count specifies the number of loops that are executed when the auto-transmit mode is enabled. If this field is a zero, the transmission continues indefinitely until disabled or the value is changed.

Index time-out specifies the number of 16 nsec clock periods added to one transmit clock period to calculate the time used to determine when a time-out occurs. This value must be increased to compensate for a longer distance between the transmitter and the receiver.

Index Tx phase specifies the phase of the operational clock on which the transmit data bit transitions. The value signifies the number of 16 nsec clock periods following the rising edge of the operational clock. This field must be less than or equal to 2n + 1, where n = clock divisor. If the 1x clock mode is being used, certain values should be avoided (clock divisor + 2 and clock divisor + 3) as they may be missing or duplicated when the phase locked loop resynchronizes to the input clock. If clock divisor = 1, only a value of 3 needs to be avoided.

Index Tx1,2 enabled when set to a one enables the use of the corresponding data register in the auto-transmit mode. When this bit is a zero the corresponding data register will not be used.

Error direction when set to a one the corresponding error signal (error1 for index1 control register etc.) is configured as an output. When this bit is a zero, the corresponding error signal is configured as an input.

Error output value determines the value of the corresponding error signal if it is configured as an output. If the signal is configured as an input, this bit has no effect.

Index auto-terminate when set to a one causes the Index line terminator to be enabled when the line is functioning as a receiver and to be disabled when the line is functioning as a transmitter regardless of the value of the terminator enable bit in the BIS2_TERM register. When this bit is a zero, the terminator is enabled by the corresponding register bit only.

Index status response specifies the three-bit status value appended to the nine-bit data word when the 12-bit response is enabled.

Index auto-transmit enable when set to a one enables the auto-transmit mode. When this mode is enabled and one or both of the index Tx1,2 bits are set, the data value(s) in these registers will be automatically sent, one value every 10 µsec if both registers are enabled the data will alternate between the two values. The loop count field determines how many times the complete loop will repeat. When this bit is zero, only discrete loads/transmissions are enabled

Index response size when set to a one enables the 12-bit response. The nine bits received are echoed and the three-bit status response is appended to generate the response data. If this bit is zero, only the nine-bit data word is echoed.

Index Tx Rx when set to a one enables the state machine to initiate a transmission (if enabled) when the appropriate configuration bits are set. When this bit is a zero, the state machine waits to receive data and then generates a response.

Index Enable when set to a one enables the Index state machine. When this bit is a zero no Index data can be transmitted or received.

BIS2_STAT0

[$18] BiSerial-II Status Port 0 read only

STATUS	
DATA BIT	DESCRIPTION
31	Response FIFO 2 data count(1)
30	Response FIFO 2 data count(0)
29	Response FIFO 1 data count(1)
28	Response FIFO 1 data count(0)
27	Response FIFO 2 data ready
26	FIFO B data ready
25	Response FIFO 1 data ready
24	Spare
23	FIFO A data ready
22	Spare input value
21	Clock select input value
20	Alive latched value
19	Error2 direction
18	Error1 direction
17	Error2 input value
16	Error1 input value
15	Interrupt Status
14	Response FIFO 2 Full
13	Response FIFO 2 Empty
12	FIFO B Full
11	FIFO B Almost Full
10	FIFO B Half Full
9	FIFO B Almost Empty
8	FIFO B Empty
7	Spare
6	Response FIFO 1 Full
5	Response FIFO 1 Empty
4	FIFO A Full
3	FIFO A Almost Full
2	FIFO A Half Full
1	FIFO A Almost Empty
0	FIFO A Empty

FIGURE 9 PMC BISERIAL-II STATUS REG 0 BIT MAP

Response FIFO 1,2 data count(1,0) are the two most significant bits of the word count of the corresponding response FIFOs. These bits signify which quarter of the FIFO is currently being accessed. If "00", the FIFO is less than a quarter full, if "01" the FIFO is between ¼ and ½ full, if "10" the FIFO is between ½ and ¾ full, and if "11" the FIFO is ¾ full or above.

When Response FIFO 1,2 data ready is read as a one, it indicates that at least one word is available to be read from the corresponding FIFO, when zero, there is no data available from the FIFO.

When FIFO A,B data ready is read as a one, it indicates that at least one word is available to be read from the corresponding FIFO, when zero, there is no data available from the FIFO.

Spare input value is the value of the Spare static I/O bit when it is configured as an input. The direction of the signal is controlled in the base control register.

Clock select input value is the value of the Clock select static I/O bit when it is configured as an input. The direction of the signal is controlled in the base control register.

Alive latched value is the value of the Alive latch bit. This latch is enabled when Alive is configured as an input, or when Alive is an output and is setup to detect a missing external clock. The latched value will be read as a one if the Alive input has gone high previously or if the external clock is missing when setup to detect it. Reading this status register will clear the latch automatically. The configuration of the Alive I/O is controlled in the base control register.

When Error1,2 direction is read as a one, the corresponding Error signal is configured as an output. When it is read as a zero, the signal is an input and the value is determined from the value bit described below.

Error1,2 input value is the value of the corresponding Error signal when it has been configured as an input. The direction of the Error signals is controlled in the corresponding Index control register.

When Interrupt Status is read as a one, it indicates that one or more latched interrupt conditions are true. In order for an actual system interrupt to occur, the interrupt enable for that condition and the Master Interrupt Enable must both be asserted. When this bit is zero, no interrupt conditions are pending.

Response FIFO 1,2 Full is read as a one, the corresponding FIFO is full; when it is a zero, the FIFO is not full.

Response FIFO 1,2 Empty is read as a one, the corresponding FIFO is empty although there could still be one more word in the read holding register (see Response FIFO 1,2 data ready). When this bit is zero there is data in the FIFO.

When FIFO A,B Full is read as a one, the corresponding FIFO is full; when it is a zero, the FIFO is not full.

When FIFO A,B Almost Full is read as a one, the corresponding FIFO is almost full as determined by the programmable offset flag registers. When this bit is zero the FIFO is below almost full.

When FIFO A,B Half Full is read as a one, the corresponding FIFO is half-full or more; when it is zero, the FIFO is below half-full.

When FIFO A,B Almost Empty is read as a one, the corresponding FIFO is almost empty as determined by the programmable offset flag registers. When this bit is zero the FIFO is above almost empty.

When FIFO A,B Empty is read as a one, the corresponding FIFO is empty although there could still be one more word in the read holding register (see FIFO A,B data ready). When this bit is zero there is data in the FIFO.

BIS2_SW_IN

[$1C] BiSerial-II Switch Read Port read only

USER CONTROL SWITCH REGISTER	
DATA BIT	DESCRIPTION
15	Rev 7
14	Rev 6
13	Rev 5
12	Rev 4
11	Rev 3
10	Rev 2
9	Rev 1
8	Rev 0
7	UB7
6	UB6
5	UB5
4	UB4
3	UB3
2	UB2
1	UB1
0	UB0

FIGURE 10 PMC BISERIAL-II SWITCH READ BIT MAP

The Switch Read Port has the user bits. The user bits are connected to the eight dipswitch positions. The switches allow custom configurations to be defined by the user and for the software to identify a particular board by its switch settings and to configure it accordingly. The silk-screen is marked with the bit positions and '0' and '1' definitions.

The upper eight bits are used to identify the revision of the Xilinx prom installed. This is useful for configuration control. The current revision is "00000101".

BIS2_INDEX1,2_DATA

[$20,$2C] BiSerial-II Index write-read ports
When the Index interface is enabled and configured to transmit first, writing a nine-bit word to the corresponding address causes the data to be loaded into the index shift register, start and stop bits added, and shifted out serially at the rate specified by the clock parameters. When the index data available bit is set in the Stat1 status register, the received data can be read from the corresponding address. This data will be a nine or twelve bit quantity, depending on the configuration of the appropriate Index interface.

BIS2_INDEX1,2_TX1

[$24,$30] BiSerial-II Index Transmit data1 write-read ports
A nine-bit word written to this address is sent when the corresponding Index interface is configured in auto-transmit mode and the Tx1 enable is set to a one. A read from these addresses simply retrieves whatever was previously written.

BIS2_INDEX1,2_TX2

[$28,$34] BiSerial-II Index Transmit data2 write-read ports
A nine-bit word written to this address is sent when the corresponding Index interface is configured in auto-transmit mode and the Tx2 enable is set to a one. A read from these addresses simply retrieves whatever was previously written.

BIS2_UART1,2_DATA

[$38,$3C] BiSerial-II UART (FIFO A,B) write-read ports
When a UART is configured as a controller, the packet data to be sent is written to the respective address, which loads it into the corresponding FIFO. If the UART is configured as a terminal, the received packets are stored in its FIFO and can be read from the corresponding address. If the FIFO loop test bit is set in the UART configuration register, the FIFO can be written and read from the appropriate address listed above.

BIS2_TERM

[$40] BiSerial-II Termination Control Register Port read/write

CONTROL TERM REGISTER		
DATA BIT	DESCRIPTION	
29-16	TERMination 13-0	1 = terminated

FIGURE 11 PMC BISERIAL-II TERMINATION CONTROL BIT MAP

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated and where. In some systems it will make sense to terminate the lines in the cable and in others it will make sense to use the onboard terminations.

The terminations for the receive groups should be set to terminate with the user software in most cases (term_10). The Index lines (I/O 3, 5) can be configured to auto-terminate so that the terminations are enabled when the line is receiving and disabled when the line is transmitting. This setting supercedes the control bits in this register.

CONTROL	CORRESPONDING IO BIT(S)
TERM_0..7	IO_0..7
TERM_8	IO_8..11
TERM_9	IO_12..15
TERM_10	IO_16..19
TERM_11	IO_20..23
TERM_12	IO_24..27
TERM_13	IO_28..31

BIS2_STAT1

[$44] BiSerial-II Status Port 1 read/write

STATUS	
DATA BIT	DESCRIPTION
31-16	Spare
15	Response FIFO 2 ¾ Full
14	Response FIFO 2 ¼ Full
13	Response FIFO 1 ¾ Full
12	Response FIFO 1 ¼ Full
11	FIFO B Almost Full
10	FIFO B Almost Empty
9	FIFO A Almost Full
8	FIFO A Almost Empty
7	UART 2 Time-out Error Detected
6	Index 2 Time-out Error Detected
5	Index 2 Framing Error Detected
4	Index 2 Data Available
3	UART 1 Time-out Error Detected
2	Index 1 Time-out Error Detected
1	Index 1 Framing Error Detected
0	Index 1 Data Available

FIGURE 12 PMC BISERIAL-II STATUS REG 1 BIT MAP

All bits in this register are latched high when the appropriate condition occurs. They will remain high until they are explicitly cleared by writing to this address with a one in the corresponding bit position.

When Response FIFO 1,2 ¾ Full is read as a one, it signifies that the respective response FIFO has become ¾ full since the bit was last cleared. This means that the FIFO was below ¾ full and then reached ¾ full or above. If the bit is read as a zero, the FIFO has not become ¾ full since the bit was last cleared.

When Response FIFO 1,2 ¼ Full is read as a one, it signifies that the respective response FIFO has become ¼ full since the bit was last cleared. This means that the FIFO was above ¼ full and then dropped to ¼ full or below. If the bit is read as a zero, the FIFO has not become ¼ full since the bit was last cleared.

When FIFO A,B Almost Full is read as a one, it indicates that the corresponding FIFO has become almost full, that is, it has gone from less than almost full to almost full or above. When this bit is a zero, the FIFO has not become almost full since the bit was last cleared.

When FIFO A,B Almost Empty is read as a one, it indicates that the corresponding FIFO has become almost empty, that is, it has gone from above almost empty to almost empty or below. When this bit is a zero, the FIFO has not become almost empty since the bit was last cleared.

When UART 1,2 Time-out Error Detected is read as a one, it indicates that a time-out error has been detected in the respective UART receiver since the bit was last cleared. This means that a packet was sent and a response was not received within one millisecond. If the bit is read as a zero this means that no time-out errors have been detected in the corresponding interface since the bit was last cleared.

When Index 1,2 Time-out Error Detected is read as a one, it indicates that a time-out error has been detected in the respective Index receiver since the bit was last cleared. This means that a data word was sent and a response was not received within the specified time (see Index configuration register description). If the bit is read as a zero this means that no time-out errors have been detected in the corresponding interface since the bit was last cleared.

When Index 1,2 Framing Error Detected is read as a one, it indicates that a framing error has been detected in the respective Index receiver since the bit was last cleared. This means that the stop bit was not read as a one. This can be caused by numerous conditions such as incorrect baud rate, false start bit detection, or noisy signals. If the bit is read as a zero this means that no framing errors have been detected in the corresponding interface since the bit was last cleared.

When Index 1,2 Data Available is read as a one, a data word has been received by the corresponding interface since the bit was last cleared. If the bit is read as a zero, no data has been received since the bit was cleared.

BIS2_DATA_READ1,2

[$48,$4C] BiSerial-II UART Read Request Data write-read register ports
Data written to this register determines the data field of a read acknowledge packet returned by the corresponding interface in response to a read request packet. This simulates a read from a memory location whose address is specified in the read request packet. Reading from this register simply returns the data that was last written.

BIS2_RESP1,2_DATA

[$50,$54] BiSerial-II UART Response Data read only FIFO ports
A read from one of these addresses reads one byte of data from the respective Response FIFO provided there is data available to be read.

Interrupts

PMC BiSerial-II interrupts are treated as auto-vectored. When the software enters into an exception handler to deal with a PMC BiSerial-II interrupt the software must read the status register to determine the cause(s) of the interrupt, clear the interrupt request(s) and process accordingly. Power on initialization will provide a cleared interrupt request and interrupts disabled.

For example, the PMC BiSerial-II Index receive state machines generate an interrupt request when a word is received and the corresponding Index data available interrupt enable and Master interrupt enable bits in the BIS2_INTEN register are set.

The interrupt is mapped to INTA on the PMC connector, which is mapped to a system interrupt when the PCI bus configures. The source of the interrupt is obtained by reading BIS2_STAT1. The status remains valid until that bit in the status register is explicitly cleared.

When an interrupt occurs, the Master interrupt enable should be cleared and the status register read to determine the cause of the interrupt. Next perform any processing needed to remove the interrupting condition, clear the latched bit and set the Master interrupt enable bit high again.

The individual enables operate after the interrupt holding latches, which store the interrupt conditions for the CPU. This allows for operating in polled mode simply by monitoring the BIS2_STAT1 register. Alternatively, the conditions of interest can be enabled, but the Master interrupt enable left disabled. Then the interrupt status bit in BIS2_STATO can be monitored. If one of the enabled conditions occurs, the interrupt status bit will be set, but unless the Master interrupt enable is set, a system interrupt will not occur.

Loop-back

The Engineering kit has reference software, which includes external loop-back tests. The tests require an external cable with the following pins connected.

RS-422 Signals

SIGNAL	OUTPUT	INPUT
UART1_2+	19	30
UART1_2-	53	64
UART2_1+	22	28
UART2_1-	56	62

RS-485 Bus Signals

SIGNAL	Input/Output	Input/Output
Index1_2 +	6	9
Index1_2 -	40	43
Error1_2 +	7	11
Error1_2 -	41	45

Static RS-485 Signals (shunt position 1)

SIGNAL	Input/Output	Input/Output
ClkSel_Spare +	1	4
ClkSel_Spare -	35	38

Static RS-485 Signals (shunt position 2)

SIGNAL	Input/Output	Input/Output
Alive_Spare +	2	4
Alive_Spare -	36	38

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC BiSerial-II. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

	-12V[unused]	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 13 PMC BISERIAL-II PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC BiSerial-II. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V[unused]		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 14 PMC BISERIAL-II PN2 INTERFACE

BiSerial-II NG1 Front Panel IO Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC BiSerial-II NG1. Also, see the User Manual for your carrier board for more information. GND* is a plane which is tied to GND through a 1206 0Ω resistor. DC, AC or open are coupling options. For a customized version, or other options, contact Dynamic Engineering.

IO_0p [CLK_SEL+]	IO_0m [CLK_SEL-]	1	35
IO_1p [ALIVE+]	IO_1m [ALIVE-]	2	36
IO_20p	IO_20m	3	37
IO_2p [SPARE+]	IO_2m [SPARE-]	4	38
IO_21p	IO_21m	5	39
IO_3p [INDEX1+]	IO_3m [INDEX1-]	6	40
IO_4p [ERROR1+]	IO_4m [ERROR1-]	7	41
IO_22p	IO_22m	8	42
IO_5p [INDEX2+]	IO_5m [INDEX2-]	9	43
IO_23p	IO_23m	10	44
IO_6p [ERROR2+]	IO_6m [ERROR2-]	11	45
IO_7p	IO_7m	12	46
IO_24p	IO_24m	13	47
IO_8p [CLK_OUT1+]	IO_8m [CLK_OUT1-]	14	48
IO_25p	IO_25m	15	49
IO_9p [CLK_OUT2+]	IO_9m [CLK_OUT2-]	16	50
IO_10p [INDEX1_DIR+]	IO_10m [INDEX1_DIR-]	17	51
IO_26p	IO_26m	18	52
IO_11p [TX_UART1+]	IO_11m [TX_UART1-]	19	53
IO_27p	IO_27m	20	54
IO_12p [INDEX2_DIR+]	IO_12m [INDEX2_DIR-]	21	55
IO_13p [TX_UART2+]	IO_13m [TX_UART2-]	22	56
IO_28p	IO_28m	23	57
IO_14p	IO_14m	24	58
IO_29p	IO_29m	25	59
IO_15p	IO_15m	26	60
IO_30p	IO_30m	27	61
IO_16p [RX_UART1+]	IO_16m [RX_UART1-]	28	62
IO_31p	IO_31m	29	63
IO_17p [RX_UART2+]	IO_17m [RX_UART2-]	30	64
GND*	GND*	31	65
IO_18p [CLK_IN+]	IO_18m [CLK_IN-]	32	66
GND*	GND*	33	67
IO_19p	IO_19m	34	68

FIGURE 15 PMC BISERIAL-II NG1 FRONT PANEL INTERFACE

PMC Pn4 User Interface Pin Assignment

The figure provides the pin assignments for the PMC BiSerial-II NG1 Module routed to Pn4. Also, see the User Manual for your carrier board for more information.

IO_0p	CLK_SEL+	IO_0m	CLK_SEL-	1	2
IO_1p	ALIVE+	IO_1m	ALIVE-	3	4
IO_2p	SPARE+	IO_2m	SPARE-	5	6
IO_3p	INDEX1+	IO_3m	INDEX1-	7	8
IO_4p	ERROR1+	IO_4m	ERROR1-	9	10
IO_5p	INDEX2+	IO_5m	INDEX2-	11	12
IO_6p	ERROR2+	IO_6m	ERROR2-	13	14
IO_7p		IO_7m		15	16
IO_8p	CLK_OUT1+	IO_8m	CLK_OUT1-	17	18
IO_9p	CLK_OUT2+	IO_9m	CLK_OUT2-	19	20
IO_10p	INDEX1_DIR+	IO_10m	INDEX1_DIR-	21	22
IO_11p	TX_UART1+	IO_11m	TX_UART1-	23	24
IO_12p	INDEX2_DIR+	IO_12m	INDEX2_DIR-	25	26
IO_13p	TX_UART2+	IO_13m	TX_UART2-	27	28
IO_14p		IO_14m		29	30
IO_15p		IO_15m		31	32
IO_16p	RX_UART1+	IO_16m	RX_UART1-	33	34
IO_17p	RX_UART2+	IO_17m	RX_UART2-	35	36
IO_18p	CLK_IN+	IO_18m	CLK_IN-	37	38
IO_19p		IO_19m		39	40
IO_20p		IO_20m		41	42
IO_21p		IO_21m		43	44
IO_22p		IO_22m		45	46
IO_23p		IO_23m		47	48
IO_24p		IO_24m		49	50
IO_25p		IO_25m		51	52
IO_26p		IO_26m		53	54
IO_27p		IO_27m		55	56
IO_28p		IO_28m		57	58
IO_29p		IO_29m		59	60
IO_30p		IO_30m		61	62
IO_31p		IO_31m		63	64

FIGURE 16 PMC BISERIAL-II PN4 INTERFACE

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. The pin definitions are defined with noise immunity in mind. The pairs are chosen to match standard SCSI II/III cable pairing to allow a low cost commercial cable to be used for the interface.

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PMC BiSerial-II when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels is recommended.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. The PMC BiSerial-II does not contain special input protection. The connector is pinned out for a standard SCSI II/III cable to be used. The twisted pairs are defined to match up with the BiSerial-II pin definitions. It is suggested that this standard cable be used for most of the cable run.

Terminal Block. We offer a high quality 68-screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68
[http://www.dyneng.com/HDEterm68.html]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the RS-485 devices rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC BiSerial-II is constructed out of 0.062 inch thick FR4 material.

Through hole and surface mounting of components are used. IC sockets use screw machine pins. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BiSerial-II design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than two Watts is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Dynamic Engineering warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, Dynamic Engineering's sole responsibility shall be to repair, or at Dynamic Engineering's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to Dynamic Engineering. All replaced products become the sole property of Dynamic Engineering.

Dynamic Engineering's warranty of and liability for defective products is limited to that set forth herein. Dynamic Engineering disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering, contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
support@dyneng.com

Specifications

Host Interface:	PCI Mezzanine Card - 32 bit
Serial Interface:	RS-485: Tx_UART1, Rx_UART1, Tx_UART2, Rx_UART2, Index1, Index2, Error1, Error2, Index1_dir, Index2_dir, Clk_sel, Alive, Spare, Clk_out1, Clk_out2, Clk_in
UART and Index Data rates:	15.625, 10.417, 7.8125, 6.25, 5.208, 4.464, 3.906 MHz with 31.25 MHz oscillator. Other rates are available with different oscillator installation.
Software Interface:	Control Registers, Status Ports, FIFOs
Initialization:	Hardware Reset forces all registers to 0.
Access Modes:	LW boundary Space (see memory map)
Wait States:	1 for all addresses
Interrupt:	FIFO A,B Almost Full FIFO A,B Almost Empty Index 1,2 Data Available Index 1,2 Framing Error Detected Index 1,2 Time-out Error Detected UART 1,2 Time-out Error Detected Response FIFO 1,2 ¼ Full Response FIFO 1,2 ¾ Full
DMA:	No DMA Support implemented at this time
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module.
Construction:	FR4 Multi-Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V

Order Information

PMC BiSerial-II NG1	PMC Module with 2 Full Duplex UART channels, 2 Half Duplex Index channels, 2 Index Direction Outputs, 2 Bi-Directional Error signals, 3 Bi-Directional Static I/O signals, 2 Clock Output ports, and 1 Clock Input Port
Eng Kit–PMC BiSerial-II	HDEterm68 – 68-position screw terminal adapter http://www.dyneng.com/HDEterm68.html HDEcabl68 - 68 IO twisted pair cable http://www.dyneng.com/HDEcabl68.html Technical Documentation, 1. PMC BiSerial-II Schematic 2. PMC BiSerial-II NG1 Reference test software Data sheet reprints are available from the manufacturer's web site reference software: C source code requires driver.

***Note**: The Engineering Kit is strongly recommended for first time* PMC BiSerial-II *purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.