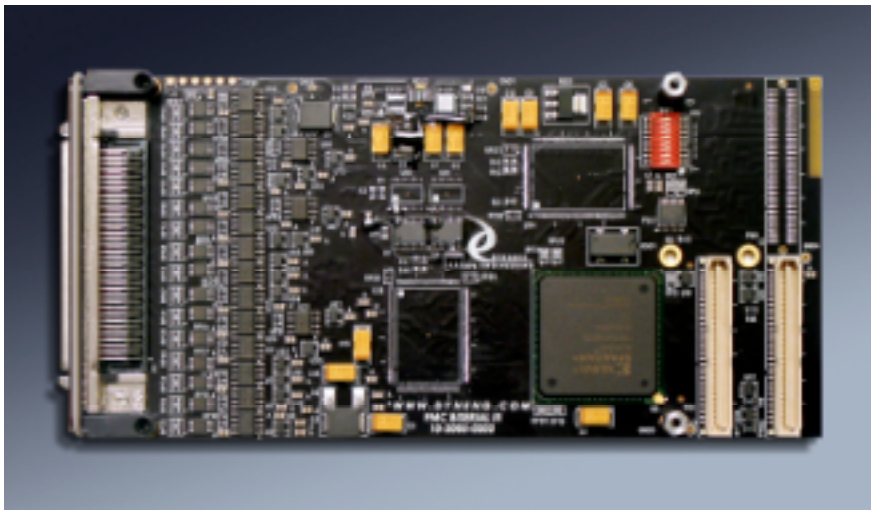
DYNAMIC ENGINEERING
150 DuBois St. Suite C, Santa Cruz, CA 95060
831-457-8891 Fax 831-457-4793
http://www.dyneng.com
sales@dyneng.com
Est. 1988

User Manual

PMC-BiSerial-III-BA19

Digital Parallel Interface
PMC Module
Master and Target Data Extraction Interface Protocols
LVDS



Revision A1
Corresponding Hardware: Revision 1
10-2005-0204
FLASH 0A02

PMC-BiSerial-III-BA19

Digital Parallel Interface
PMC Module
Dynamic Engineering
150 DuBois St. Suite C, Santa Cruz CA 95060
831-457-8891 831-457-4793 FAX

Dynamic Engineering has made every effort to ensure that this manual is accurate and complete. Still, the company reserves the right to make improvements or changes in the product described in this document at any time and without notice. Furthermore, Dynamic Engineering assumes no liability arising out of the application or use of the device described herein.

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Dynamic Engineering's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Dynamic Engineering.

This product has been designed to operate with PMC Module carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

Manual Revision A1. Revised 3/2/09

Table of Contents

List of Figures

Product Description

In embedded systems many of the interconnections are made with differential [RS-422/485 or LVDS] signals. Depending on the system architecture an IP or a PMC will be the right choice to make the connection. You have choices with carriers for cPCI, PCI, VME, PC/104p and other buses for both PMC and IP mezzanine modules.

Usually the choice is based on other system constraints as both the PMC and IP can provide the IO you require. Dynamic Engineering would be happy to assist in your decision regarding architecture and other trade-offs with the PMC / IP decision. Dynamic Engineering has carriers for IP and PMC modules for most systems, and is adding more as new solutions are requested by our clients.

The PMC compatible PMC-BiSerial-III has 34 independent differential IO available. The high density makes efficient use of PMC slot resources. The IO is available for system connection through the front panel [34], via the rear [Pn4] connector [32], or both. A high density 68 pin SCSI III front panel connector provides the front panel IO. The rear panel IO has a PIM and PIM Carrier available for rear panel wiring options.

PMC-BiSerial-III-BA19 is a “clientized” version of the standard PMC-BiSerial-III board. “BA19” is set to use the LVDS standard, has front panel IO, and supports one Master and one Target channel. The PLL is programmed for the base clock rate that the Master interface will use to transfer data with a Target. The PLL is referenced to 50 MHz. and can be programmed with new .JED files using the driver.

The data is transferred as byte wide with a reference clock, ready and sync signal. The Target requests a transfer by raising the READY signal. The Master responds when enabled with the reference clock. Data is transferred using both edges of the clock. The Target using the rising edge and the Master sampling on the falling edge. Sync is asserted for the first byte and for the start of each block of data that follows. A block is always a LW sized byte count [4,8 etc.] and usually set to 2048.

The Master and Target interfaces have programmable block counts. The Target transmits based on the block count and the Master does error checking based on the expected size. The Master will continue to receive even with sync position errors, and the error status bit will be set.

DMA or single word accesses can be used to load and unload the FIFO’s. 8K x 32 FIFO’s are used for the Master and Target. The Dynamic Driver supports both modes of operation.

The Master and Target can be used in pairs for loop-back testing. HDEterm68 http://www.dyneng.com/HDEterm68.html can be used as a breakout for the front panel IO. The HDEcabl68 provides a convenient cable.

http://www.dyneng.com/HDEcabl68.html Custom cables can be manufactured to your requirements. The loop-back IO definitions are toward the end of this manual. Please contact Dynamic Engineering with your specifications.

In this design the Termination and Direction controls are set in the VHDL. The received signals are terminated and the transmitted signals are not.

All of the IO are routed through the FPGA to allow for custom applications that require hardware intervention or specific timing- for example an automatic address or data strobe to be generated. The initial model was register based [FLASH 0101]. Please contact Dynamic Engineering with your custom requirements. BA19 is design number "A" for the PMC-BiSerial-III with a corresponding FLASH of 0Axx.

The IO are buffered from the FPGA with differential transceivers. The transceivers can be populated with LVDS or RS-485 compatible devices. The power plane for the transceivers is isolated to allow selectable 3.3 or 5V references for the IO. The LVDS IO requires 3.3 and 40 MHz capable RS-485 requires 5V. When mixed LVDS and RS485 are used the reference is set to 3.3 and lower speed RS-485 parts are used that are compatible with the 3.3V.

The IO are matched from the connector edge to the ball on the FPGA. The differential side is routed with controlled impedance traces. "Trace and space".

Each of the transceivers has separate direction and termination controls to allow for Any configuration of in and out, half and full duplex designs.

Each of the IO has series terminations to allow the IO to be isolated or terminated. The isolation feature is used to allow rear or front panel implementations without "stub" issues for higher speed signals.

Each IO has pull-up and pull-down options to allow half duplex lines to be set to a "marking" state when no device is on the line. The P is is ganged and the M side is too. Each side can be set to gnd or vcc to allow a '1' or a '0' to be set on the lines. The resistors are in resistor packs and can be implemented with many values.

The terminations utilize analog switches to selectively parallel terminate the differential pair with approximately 100 ohms. It is recommended that the receiver side provide the termination.

The analog switches are protected with a DIODE on the input side of the power supply. The switches can back-feed voltage into the rest of the circuit when the PMC is powered down and the system connected to it is not. The DIODE's allow for more flexible operation and power sequencing.

The registers are mapped as 32 bit words and support 32 bit access. Most registers are read-writeable. The Windows® compatible driver is available to provide the system level interface for this version of the Biserial III. Use standard C/C++ to control your hardware or use the Hardware manual to make your own software interface. The software manual is also available on-line. Linux is available by request.

PMC-BISERIAL-III is part of the PMC Module family of modular I/O components. The PMC-BISERIAL-III conforms to the PMC standard. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, with final system implementation on a different one.

PMC-BISERIAL-III can be used for multiple purposes with applications in telecommunications, control, sensors, IO, test; anywhere multiple independent or coordinated IO are useful.

PMC-BISERIAL-III features a Xilinx FPGA, and high speed differential devices. The FPGA contains the PCI interface and control required for the parallel interface.

The Xilinx design incorporates the “PCI Core” and additional modules for DMA in parallel with a direct register decoded programming model. The design model has a “base” level with the basic board level functions and “channels” which contain IO oriented functions. In the BA19 design the COM functions are designed into channels and the PLL programming, switch, and other common or basic functions are in the base design.

From a software perspective the design can be treated as “Flat” or as a hierarchy. The Dynamic Engineering Windows® driver uses the hierarchical approach to allow for more consistent software with common bit maps and offsets. The user software can control the COM pairs with the same calls and use the channel number to distinguish. This makes for consistent and easier to implement user level software.

The hardware is designed with each of the channels on a common address map – each channel has the same memory allocated to it and as much as possible the offsets within each space are defined in the same way or similar way. Again this make understanding each port easier to accomplish and less likely to have errors.

The transceivers are initialized to the receive state. Once a channel is defined via software to be a transmitter the IO are enabled and driven to the appropriate levels. Terminations are activated for ports defined to be receivers.

All the IO control and registers are instantiated within the FPGA, only the transceivers and termination switches are separate devices. If desired, the IO lines can be specially programmed to create custom timing pulses etc. Please contact Dynamic Engineering with your requirements.

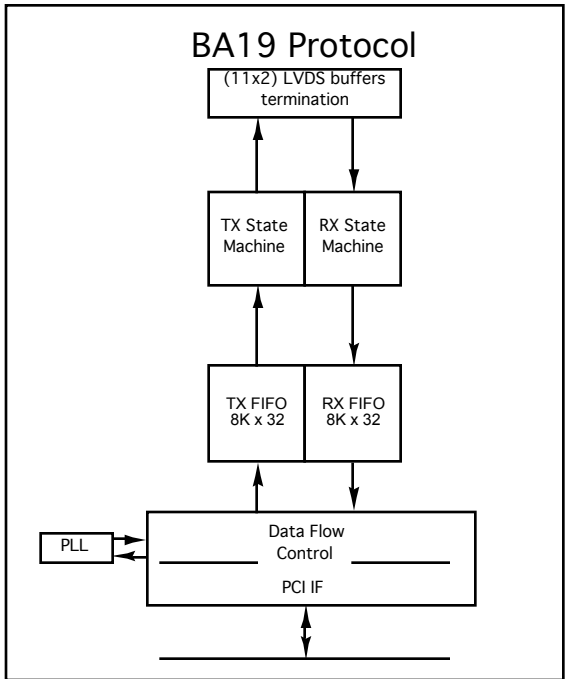


Figure 1 PMC-BISERIAL-III-BA19 Block Diagram

PMC BiSerial III BA19 features a Master and a Target port with DMA support. The internal block RAM is configured to provide FIFO's to support the DMA and IO transfer process. 8K x 32 per port. The Target transmits the data to the Master at the request of the master.

The Master port supplies the clock and the Target supplies Ready, Strobe and Data. The Target asserts Ready when data is ready to transfer. The Master responds by driving the clock. The clock can be stopped if the Master needs to hold off the transfer of data. Ready is not asserted unless there is sufficient data in the FIFO to complete the transfer. Data is send in parallel words, 8 bits per clock. Every block the sync signal is asserted. The size of the data is "agreed to" in the controlling software ahead of the transfer taking place.

The hardware will pull data from the FIFO memory and store into the system memory using DMA and vice-versa. The transfer function will load the FIFO and DMA will unload. The DMA function operates at the PCI bus frequency. The transfer frequency will determine the maximum load rate into the FIFO.

The DMA programmable length is 32 bits => longer than most computer OS will allow in one segment of memory. The DMA is scatter gather capable for longer lengths than the

OS max and for OS situations where the memory is not contiguous. With Windows® lengths of 4K are common while Linux can provide much larger spaces. Larger spaces are more efficient as there are fewer initialization reads and reduced overhead on the bus. A single interrupt can control the entire transfer. Head to tail operation can also be programmed with two memory spaces with two interrupts per loop.

The hardware is organized with the IO function in channel 0 and the card level functions in the “base”. The driver provides the ability to find the hardware and to allocate resources to use the base and channel functions.

The basic use of the interface is to capture data from an external device and to store into a file on a hard drive. The driver and reference application provide a mechanism to create a file on the hard drive and to use DMA to move the data from the external device to the file. In addition loop-back testing can be done between the Target and Master channels.

The base rate is 1.932 Mbytes per second. The HW default is set to this rate for convenience. The PLL can be used to program alternate rates of operation.

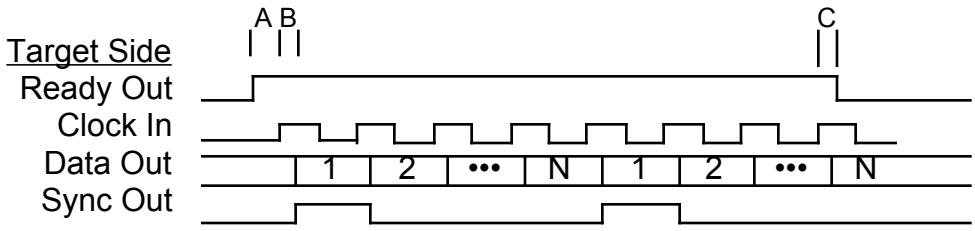


Figure 2 PMC-BISERIAL-III-BA19 Timing Diagram

Target side timing is shown. Assuming the standard rate clock, the period will be 518 – 521 nS. The minimum delay “A” from Ready Out to Clock In is 50 nS. Master can hold off clock for an extended delay. Rising edge received to Sync Out and Data Out “B” is 80 nS delay max. Last clock in Block to Ready Out disabled delay “C” is 80 nS Max.

Sync Out is asserted for the first byte in each block.

Bytes are numbered based on PCI Little Endian conventions – D7–0 on the PCI bus become Byte 1, D15 – 8 become Byte 2 etc. Both for transmission and for reception – data packing before transfer to host memory. A control bit is available to swap ends and operate from D31 –24. Please refer to the bitmaps for more information.

Address Map

Function	Offset
// **PMC BiSerial III BA19 definitions**	
#define BA19_BASE_BASE	0x0000 // 0 BA19Base Base control register
#define BA19_BASE_PLL_WRITE	0x0000 // 0 BA19Base Base control register
#define BA19_BASE_PLL_READ	0x0000 // 0 BA19Base base control register
#define BA19_BASE_USER_SWITCH	0x0004 // 1 BA19Base User switch read port DIP switch read
#define BA19_BASE_XILINX_REV	0x0004 // 1 BA19Base Xilinx revision read port
#define BA19_BASE_XILINX_DES	0x0004 // 1 BA19Base Xilinx design read port
#define BA19_BASE_STATUS	0x0008 // 2 BA19Base status Register offset

Figure 3 PMC-BISERIAL-III Internal Address Map Base Functions

The address map provided is for the local decoding performed within PMC-BiSerial-III. The addresses are all offsets from a base address. The carrier board that the PMC is installed into provides the base address. Dynamic Engineering prefers a long-word oriented approach because it is more consistent across platforms.

The map is presented with the #define style to allow cutting and pasting into many compilers “include” files.

The host system will search the PCI bus to find the assets installed during power-on initialization. The VendorId = 0x10EE and the CardId = 0x0038 for the PMC-BiSerial-III-BA19.

The BA19 design has 1 channel implemented at this time. The BASE contains the common elements of the design, while the Channels have the IO specific interfaces. The BASE starts at the card offset. Channel 0 starts at register 28

Section	Register Address Range (starting Hex address)	COM name
Base	0-27 (0x0000)	PLL, Switch, Status
Channel 0	28-41 (0x0070)	BA19 Master and Target

Function	Offset from Channel Base Address
// PMC BiSerial III BA19 Channel definitions	
#define BA19_CHAN_CNTRL	0x0000 //0 BA19Chan General control register
#define BA19_CHAN_MASTER_CNTL	0x0004 //1 BA19Chan Master Control Port
#define BA19_CHAN_TARGET_CNTL	0x0008 //2 BA19Chan Target Control Port
#define BA19_CHAN_INT_STATUS	0x000C //3 BA19Chan Interrupt status port
#define BA19_CHAN_INT_CLEAR	0x000C //3 BA19Chan Interrupt clear port
#define BA19_CHAN_WR_DMA_PNTR	0x0010 //4 BA19Chan Write DMA dpr[1] physical PCI add
#define BA19_CHAN_RD_DMA_PNTR	0x0014 //5 BA19Chan Read DMA dpr physical PCI add
#define BA19_CHAN_FIFO	0x0018 //6 BA19Chan FIFO single word access
#define BA19_CHAN_MASTER_AFL_LVL	0x001C //7 BA19Chan Master almost full level register
#define BA19_CHAN_TARGET_AMT_LVL	0x0020 //8 BA19Chan Target almost empty level register
#define BA19_CHAN_TARGET_FIFO_COUNT	0x0024 //9 BA19Chan Target FIFO count read port
#define BA19_CHAN_MASTER_FIFO_COUNT	0x0028 //10 BA19Chan Master FIFO count + pipeline
#define BA19_CHAN_MASTER_COUNT	0x002C //11 BA19Chan MasterCount
#define BA19_CHAN_TARGET_COUNT	0x0030 //12 BA19Chan TargetCount
#define BA19_CHAN_MASTER_INT_LEVEL	0x0034 // 13 BA19Chan MasterIntLevel

Figure 4 PMC-BISERIAL-III Channel Address Map

[1] **DPR = Descriptor Pointer and is the physical location of the descriptor in host memory**

Programming

Programming the PMC-BISERIAL-III-BA19 requires only the ability to read and write data in the host's PMC space.

Once the initialization process has occurred, and the system has assigned addresses to the PMC-BiSerial-III-BA19 card the software will need to determine what the address space is for the PCI interface [BAR0]. The offsets in the address tables are relative to the system assigned BAR0 base address.

The next step is to initialize the PMC-BiSerial-III-BA19. The PLL will need to be programmed to use the BA19 function. The Cypress CyberClocks software can be used to create new .JED files if desired. The PLLA should be set to the transmit reference frequency output by the Master.

The driver comes with several .JED files prepared. The driver has a utility to load the PLL and read back. The reference application software has an example of the use of PLL programming. The reference application software also includes XLATE.c which converts the .JED file from the CyberClocks tool to an array that can be programmed into the PLL.

The IO direction and termination are hardwired in this design. The ports are unidirectional and initialization is simplified with this approach.

The control bits will select how the data is transmitted – Byte ordering, size of transfer etc.

For Windows™ and Linux systems the Dynamic Drivers[2] can be used. The driver will take care of finding the hardware and provide an easy to use mechanism to program the hardware. The Driver comes with reference software showing how to use the card and reference frequency files to allow the user to duplicate the test set-up used in manufacturing at Dynamic Engineering. Using simple, known to work routines is a good way to get acquainted with new hardware.

To use the BA19 specific functions the Channel Control, and PLL interface plus DMA will need to be programmed. To use DMA, memory space from the system should be allocated and the link list stored into memory. The location of the link list is written to the BA19 to start the DMA. Please refer to the Burst IN and Burst Out register discussions.

[2] Currently only Windows® is supported. Please contact Dynamic Engineering for Linux.

DMA should be set-up before starting the channel port function. For transmission this will result in the FIFO being full or close to it when the transfer is started. For reception it means that the FIFO is under HW control and the delay from starting reception to starting DMA won't cause an overflow condition.

DMA can be programmed with a specific length. The length can be as long as you want within standard memory limitations. At the end of the DMA transfer the Host will receive an interrupt. The receiver can be stopped and the FIFO reset to clear out any extra data captured. For on-the-fly processing multiple shorter DMA segments can be programmed; at the interrupt restart DMA to point at the alternate segment to allow processing on the previous one. This technique is sometimes referred to as "ping-pong".

Base Register Definitions

BA19_BASE_BASE

[$00 parallel-io Control Register Port read/write]

DATA BIT	DESCRIPTION
31-21	spare
20	bit 19 read-back of pll_dat register bit
19	pll_dat [write to PLL, read-back from PLL]
18	pll_s2
17	pll_sclk
16	pll_en
15-2	spare
1	IntForce
0	MasterIntEn

Figure 5 PMC-BISERIAL-III Control Base Register Bit Map

This is the base control register for the PMC BiSerial III BA19. The features common to all channels are controlled from this port. Unused bits are reserved for additional new features. Unused bits should be programmed '0' to allow for future commonality.

pll_en: When this bit is set to a one, the signals used to program and read the PLL are enabled.

pll_sclk/pll_dat : These signals are used to program the PLL over the I^2C serial interface. Sclk is always an output whereas Sdata is bi-directional. This register is where the Sdata output value is specified or read-back.

pll_s2: This is an additional control line to the PLL that can be used to select additional pre-programmed frequencies. Set to '0' for most applications.

The PLL is programmed with the output file generated by the Cypress PLL programming tool. [CY3672 R3.01 Programming Kit or CyberClocks R3.20.00 Cypress may update the revision from time to time.] The .JED file is used by the Dynamic Driver to program the PLL. Programming the PLL is fairly involved and beyond the scope of this manual. For clients writing their own drivers it is suggested to get the Engineering Kit for this board including software, and to use the translation and programming files ported to your environment. This procedure will save you a lot of time. For those who want to do it themselves the Cypress PLL in use is the 22393. The output file from the Cypress tool can be passed directly to the Dynamic Driver [Linux or Windows] and used

to program the PLL without user intervention.

The reference frequency for the PLL is 50 MHz.

IntForce when set and **MasterIntEn** is also set will cause an interrupt to the host. This function is repeated in the channel. With only a single channel this function is somewhat redundant. It is suggested to use the channel based force interrupt for development since the status will be closer to operation. Please note that MasterIntEn is not required for the channel interrupts to be propagated to the host.

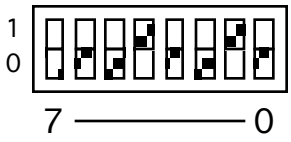
BA19_BASE_ID

[$04 Switch and Design number port read only]

DATA BIT	DESCRIPTION
31-24	spare
23-8	Design ID and Revision
7-0	DIP switch

Figure 6 PMC-BISERIAL-III ID and Switch Bit Map

The DIP Switch is labeled for bit number and '1' '0' in the silk screen. The DIP Switch can be read from this port and used to determine which PMC BiSerial III physical card matches each PCI address assigned in a system with multiple cards installed. The DIPswitch can also be used for other purposes – software revision etc. The switch shown would read back 0x12.



The Design ID and Revision are defined by a 16 bit field allowing for 256 designs and 256 revisions of each. The BA19 design is 0x0A the current revision is 0x02.

The PCI revision is updated in HW to match the design revision. The board ID will be updated for major changes to allow drivers to differentiate between revisions and applications.

BA19_BASE_STATUS

[$08 Board level Status Port read only]

DATA BIT	DESCRIPTION
31	Interrupt Status
30-17	Set to ‘0’
16	Masked Channel 0 Interrupt
15	Masked Base Interrupt
14-1	set to ‘0’
0	Unmasked Base Interrupt

Figure 7 PMC-BISERIAL-III Status Port Bit Map

Channel Interrupt – The local masked interrupt status from the channel. Each channel can have different interrupt sources. DMA Write or DMA Read or IntForce or TX/RX request are typical sources. Polling can be accomplished using the channel status register and leaving the channel interrupt disabled.

Interrupt Status – Set if the PCI interrupt is asserted. These bits can be checked to determine if this card is causing an interrupt to the system. If set the other bits can be checked to see which feature(s) of the board need to be serviced. Secondary reads to the Channel status registers will determine the exact type of interrupt. Software can implement any priority scheme desired when dealing with multiple interrupts.

Base Interrupt – Set if the base features are requesting an interrupt. The Masked version is after the enable has been applied and the Unmasked version is before the mask is applied to allow for polling.

Channel Bit Maps
The BA19 design has 1 channels. The basic control signals are the same for the channel base, channel status, FIFO and DMA interfaces. The following descriptions will be in the form of a common feature description for each address and then differences if any for each channel.

Notes:
The offsets shown are relative to the channel base address not the card base address.

BA19_CHAN_CNTRL

[0x0] Channel Control Register (read/write)

Channel Control Register

Data Bit	Description
31-7	spare
12	*reserved this design* FIFO External Reset
11-9	Spare
8	*reserved this design* OutUrgent
7	*reserved this design* InUrgent
6	Read DMA Interrupt Enable
5	Write DMA Interrupt Enable
4	Force Interrupt
3	Channel Interrupt Enable
2	Bypass
1	Master FIFO Reset
0	Target FIFO Reset

Figure 8 PMC-BISERIAL-III channel Control Register

FIFO Master/Target Reset: When set to a one, the transmit and/or receive FIFOs will be reset. When these bits are zero, normal FIFO operation is enabled. In addition the Master and Target State Machine is also reset.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA writes and reads respectively.

Channel Interrupt Enable: When this bit is set to a one, all enabled interrupts (except the DMA interrupts) will be gated through to the PCI interface level of the design; when this bit is a zero, the interrupts can be used for status without interrupting the host. The channel interrupt enable is for the channel level interrupt sources only.

Force Interrupt: When this bit is set to a one, a system interrupt will occur provided the Channel Interrupt and master interrupt enables are set. This is useful for interrupt testing.

InUrgent / OutUrgent when set causes the DMA request to have higher priority under certain circumstances. Basically when the TX FIFO is almost empty and InUrgent is set the TX DMA will have higher priority than it would otherwise get. Similarly if the RX FIFO is almost full and OutUrgent is set the read DMA will have higher priority. The purpose is to allow software some control over how DMA requests are processed and to allow for a higher rate channel to have a higher priority over other lower rate channels.

Since there is only one channel implemented this feature has been "tied off" for the BA19 design.

ByPass when set allows the FIFO to be used in a loop-back mode internal to the device. A separate state-machine is enabled when ByPass is set and the TX and RX are not enabled. The state-machine checks the TX and RX FIFO's and when not empty on the TX side and not Full on the RX side moves data between them. Writing to the TX FIFO allows reading back from the RX side. An example of this is included in the Driver reference software.

FIFO External Reset: When cleared to a zero, the External FIFOs will be reset. When set the External FIFO is enabled. The HS channels have external 128Kx32 FIFO's attached. Please note that the state of the Load pin in the transmit control register affects how the part comes out of reset – what the default Almost Full and Almost Empty offsets are.

This function is reserved since the BA19 design does not use external FIFO's.

BA19_MASTER_CNTRL

[0x04] Channel Master Control Register (read/write)

Channel Control Register

Data Bit	Description
15-3	spare
2	MasterLvlInt
1	MasterEndian
0	MasterEn

Figure 9 PMC-BISERIAL-III Channel Master Control Register

MasterEn when set causes the Master State Machine to begin operation. If the Target is waiting to transfer data with the Ready Out set the Master will begin to send clocks. If the Target is not ready, the Master will be enabled, but wait for the Target to begin the transfer.

MasterEndian when cleared stores the first byte received onto the D7-0 lane in the FIFO and PCI bus. D15-8 is second and D31-24 last. If the control bit is set the order is reversed causing D31-24 to be loaded with the first byte received and D7-0 with the 4th byte received.

MasterLvlInt when set enables the interrupt based on the Master FIFO Almost full flag. When the interrupt occurs a programmable amount of data is stored into the FIFO making for an efficient DMA read or burst of reads to unload the FIFO.

BA19_TARGET_CNTRL

[0x08] Channel Master Control Register (read/write)

Channel Control Register

Data Bit	Description
15-3	spare
2	TargetLvlInt
1	TargetEndian
0	TargetEn

Figure 10 PMC-BISERIAL-III Channel Target Control Register

TargetEn when set causes the Target State Machine to begin operation. The FIFO is tested and assuming not empty, the ReadyOut signal will be asserted. If the Master is

ready to transfer data it will assert clocks to begin the transfer.

TargetEndian when cleared transmits the first byte from the D7-0 lane in the FIFO and PCI bus. D15-8 is second and D31-24 last. If the control bit is set the order is reversed causing D31-24 to be transmitted as the first byte and D7-0 as the 4th byte transmitted.

TargetLvlInt when set enables the interrupt based on the Target FIFO Almost Empty flag. When the interrupt occurs a programmable amount of data can be stored into the FIFO making for an efficient DMA write or burst of writes to unload the FIFO.

BA19_CHAN_STATUS

[0xC] Channel Status Read/Clear Latch Write Port

Channel Status Register

Data Bit	Description
31	Interrupt Status
30	TargetLvlIntMasked
29	MasterLvlIntMasked
28-20	Spare
19	BurstInIdle
18	BurstOutIdle
17	TargetIdleState
16	MasterIdleState
15	Read DMA Interrupt Occurred
14	Write DMA Interrupt Occurred
13	Read DMA Error Occurred
12	Write DMA Error Occurred
11	MasterFifoErrLat
10	MasterSyncErrLat
9	TargetFifoErrLat
8	Spare
7	MasterFifoAFLInt
6	Master FIFO Full
5	Master FIFO Almost Full
4	Master FIFO Empty
3	Spare
2	Target FIFO Full
1	Target FIFO Almost Empty
0	Target FIFO Empty

Figure 11 PMC-BiSerial-III Channel STATUS PORT

BA19 FIFO: Two 8K x 32 FIFO's are used to create the internal Target and Master memory. The status for the Target FIFO and Master FIFO refer to these FIFO's. The status is active high. 0x13 would correspond to empty Target and empty Master internal FIFO's.

Please note with the Master side status; the status reflects the state of the FIFO and does not take the 4 deep pipeline into account. For example the FIFO may be empty and there may be valid data within the pipeline. The data count with the combined FIFO and pipeline value and can also be used for read size control. [see later in register descriptions]

Master FIFO Empty: When a one is read, the FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Master FIFO Almost Full: When a one is read, the number of data words in the data FIFO is greater than the value written to the corresponding Master_AFL_LVL register; when a zero is read, the FIFO level is less than that value.

Master FIFO Full: When a one is read, the receive data FIFO is full; when a zero is read, there is room for at least one more data-word in the FIFO. If the FIFO is full when time to write received data to the FIFO an overflow error is declared.

Target FIFO Empty: When a one is read, the FIFO contains no data; when a zero is read, there is at least one data word in the FIFO. If the FIFO is empty when time to read transmitted data from the FIFO an underflow error is may be declared.

Target FIFO Almost Empty: When a one is read, the number of data words in the data FIFO is less than or equal to the value written to the corresponding Target_AMT_LVL register; when a zero is read, the FIFO level is more than that value.

Target FIFO Full: When a one is read, the receive data FIFO is full; when a zero is read, there is room for at least one more data-word in the FIFO.

MasterFifoErrLat When a one is read, an error has been detected. This will occur if FIFO is full when the loader function tries to write to it. A zero indicates that no error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in the appropriate bit position. This bit should never be set due to the HW holding off the clock if the FIFO is almost full.

MasterSyncErrLat When a one is read, an error has been detected. This will occur if the Master count of received bytes per block does not match the programmed quantity. Sync is tested to be set when the block boundaries indicate that it should be. Usual cause is the Target and Master not sharing a common size for the block definition.

TargetFifoErrLat When a one is read, an error has been detected. This will occur if FIFO is empty when the state machine tries to read from it. A zero indicates that no error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in the appropriate bit position. This bit should never be set due to the HW holding off the ReadyOut signal if the FIFO is almost empty.

Write/Read DMA Error Occurred: When a one is read, a write or read DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is incorrect. A zero indicates that no

write or read DMA error has occurred. These bits are latched and can be cleared by writing back to the Status register with a one in the appropriate bit position.

Write/Read DMA Interrupt Occurred: When a one is read, a write/read DMA interrupt is latched. This indicates that the scatter-gather list for the current write or read DMA has completed, but the associated interrupt has yet to be processed. A zero indicates that no write or read DMA interrupt is pending.

Channel Interrupt Active: When a one is read, it indicates that a system interrupt is asserted caused by an enabled channel interrupt condition. A zero indicates that no system interrupt is pending from an enabled channel interrupt condition. Please note that the board level master interrupt enable is not needed to allow channel level interrupts to be asserted.

Target IDLE is set when the state-machine is in the idle state. When lower clock rates are used it may take a while to clean-up and return to the idle state. If SW has cleared the start bit to terminate the data transfer; SW can use the IDLE bit to determine when the HW has completed its task and returned.

Master IDLE is set when the state-machine is in the idle state. When lower clock rates are used it may take a while to clean-up and return to the idle state. If SW has cleared the start bit to terminate the transfer; SW can use the IDLE bit to determine when the HW has completed its task and returned.

BO and BI Idle are Burst Out and Burst In IDLE state status for the Receive and Transmit DMA actions. The bits will be 1 when in the IDLE state and 0 when processing a DMA. A new DMA should not be launched until the State machine is back in the IDLE state. Please note that the direction implied in the name has to do with the DMA direction – Burst data into the card for Transmit [Target] and burst data out of the card for Receive [Master].

Local Interrupt is the masked combined interrupt status for the channel not including DMA. The status is before the master interrupt enable for the channel.

Interrupt Status is the combined Local Interrupt with DMA and the master interrupt enable. If this bit is set this channel has a pending interrupt request.

FifoInt when set indicates that the Target FIFO went Almost Empty. The bit is captured and stays set until cleared by writing with the bit position set. The Almost Empty level is

programmable. Useful when using interrupts and reactive DMA transfers – when not sure how much data to write, program the level to cause an interrupt with sufficient time to refill and wait for the interrupt. The FIFO will be able to handle the Full minus Almost empty level as a DMA transfer or single word writes. The current exact count can be read from the Target FIFO count register.

BA19_CHAN_WR_DMA_PNTR
[0x10] Write DMA Pointer (write only)

BurstIn DMA Pointer Address Register

Data Bit	Description
31-2	First Chaining Descriptor Physical Address
1	direction [0]
0	end of chain

Figure 12 PMC-BiSerial-III Write DMA pointer register

This write-only port is used to initiate a scatter-gather write [TX] DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. Essentially this data acts like a chaining descriptor value pointing to the next value in the chain.

The first is the address of the first memory block of the DMA buffer containing the data to read into the device, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

All three values are on LW boundaries and are LW in size. Addresses for successive parameters are incremented. The addresses are physical addresses the HW will use on the PCI bus to access the Host memory for the next descriptor or to read the data to be transmitted. In most OS you will need to convert from virtual to physical. The length parameter is a number of bytes, and must be on a LW divisible number of bytes.

Status for the DMA activity can be found in the channel control register and channel status register.

Notes:
1. Writing a zero to this port will abort a write DMA in progress.
2. End of chain should not be set for the address written to the DMA Pointer Address Register. End of chain should be set when the descriptor follows the last length parameter.

3. The Direction should be set to ‘0’ for Burst In DMA in all chaining descriptor locations.

BA19_CHAN_RD_DMA_PNTR

[0x14] Read DMA Pointer (write only)

BurstIn DMA Pointer Address Register	
Data Bit	Description
31-2	First Chaining Descriptor Physical Address
1	direction [1]
0	end of chain

Figure 13 PMC-BiSerial-III Read DMA pointer register

This write-only port is used to initiate a scatter-gather read [RX] DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. Essentially this data acts like a chaining descriptor value pointing to the next value in the chain.

The first is the address of the first memory block of the DMA buffer to write data from the device to, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

All three values are on LW boundaries and are LW in size. Addresses for successive parameters are incremented. The addresses are physical addresses the HW will use on the PCI bus to access the Host memory for the next descriptor or to read the data to be transmitted. In most OS you will need to convert from virtual to physical. The length parameter is a number of bytes, and must be on a LW divisible number of bytes.

Status for the DMA activity can be found in the channel control register and channel status register.

Notes:

1. Writing a zero to this port will abort a write DMA in progress.
2. End of chain should not be set for the address written to the DMA Pointer Address Register. End of chain should be set when the descriptor follows the last length parameter.
3. The Direction should be set to ‘1’ for Burst Out DMA in all chaining descriptor locations.

BA19_CHAN_FIFO

[0x18] Write TX/Read RX FIFO Port

RX [Master] and TX [Target] FIFO Port	
Data Bit	Description
31-0	FIFO data word

Figure 14 PMC-BiSerial-III RX/TX FIFO Port

This port is used to make single-word accesses from the FIFO. Data read from this port will no longer be available for DMA transfers. Writing to the port loads the Target FIFO, Reading unloads the Master FIFO.

BA19_CHAN_Master_AFL_LVL

[0x1C] Master almost-full (read/write)

Master Almost-Full Level Register	
Data Bit	Description
31-16	Spare
15-0	Master FIFO Almost-Full Level

Figure 15 PMC-BiSerial-III MASTER ALMOST FULL LEVEL register

This read/write port accesses the almost-full level register. When the number of data words in the receive data FIFO is equal or greater than this value, the almost-full status bit will be set. The register is R/W for 16 bits. The mask is valid for a size matching the depth of the FIFO. 8k x32 + 4 is the Master FIFO size for a 13 bit valid count range [12-0]. The level includes the pipeline for an additional 4 locations [0x1FFF + 4 = 0x2003].

The programmed level is used by the State Machine to control when to hold off transfers due to the FIFO being close to full.

BA19_CHAN_TARGET_AMT_LVL

[0x20] Target almost-empty level (read/write)

Target Almost-Full Level Register	
Data Bit	Description
31-16	Spare
15-0	Target FIFO Almost-Empty Level

Figure 16 PMC-BiSerial-III TARGET ALMOST EMPTY LEVEL register

This read/write port accesses the almost-empty level register. When the number of data words in the transmit data FIFO is less than than this value, the almost-empty status bit will be set. The register is R/W for 16 bits. The mask is valid for a size matching the depth of the FIFO. 8k x32 is the TX FIFO for a 13 bit valid count range [12-0]. The value is used by the State Machine to determine when to hold off sending more data.

BA19_CHAN_TARGET_FIFO_COUNT

[0x24] TX [Target] FIFO data count (read only)

TX FIFO Data Count Port	
Data Bit	Description
31-14	Spare
13-0	TX Data Words Stored

Figure 17 PMC-BiSerial-III TARGET FIFO data count Port

This read-only register port reports the number of 32-bit data words in the Transmit FIFO. This design has 8192 locations possible.

BA19_CHAN_MASTER_FIFO_COUNT

[0x28] RX [Master] FIFO data count (read only)

RX FIFO Data Count Port	
Data Bit	Description
31-14	Spare
13-0	RX Data Words Stored

Figure 18 PMC-BiSerial-III MASTER FIFO data count Port

This read-only register port reports the number of 32-bit data words in the Receive FIFO plus pipeline. The maximum count is the FIFO size plus 4 = 0x2003.

BA19_CHAN_MASTER_COUNT

[0x2C] RX [Master] data count

RX Data Count Port	
Data Bit	Description
31-16	Spare
15-0	RX Data Bytes per Block

Figure 19 PMC-BiSerial-III MASTER DATA COUNT Port

This read-write register port holds the number of bytes expected to be received per block. The first byte will have the sync set and at the start of each block after. The Master will count bytes and check for sync being asserted when the next block should be started. The Sync Error bit is set if Sync is not asserted when expected.

BA19_CHAN_TARGET_COUNT

[0x30] TX [Target] data count

TX Data Count Port	
Data Bit	Description
31-16	Spare
15-0	TX Data Bytes per Block

Figure 20 PMC-BiSerial-III TARGET DATA COUNT Port

This read-write register port holds the number of bytes to transmit per block. The first byte will have the sync set and at the start of each block after. No error bit is associated with the Target side.

BA19_CHAN_MASTER_INT_LEVEL

[0x34] RX [Master] data count (read only)

Master Interrupt Level	
Data Bit	Description
31-16	Spare
15-0	TX Data Bytes per Block

Figure 21 PMC-BiSerial-III TARGET DATA COUNT Port

This register defines a second comparison against the FIFO plus Pipeline count. When the Count is greater or equal to the programmed amount the MasterFifoAFLInt signal is set causing an interrupt to the host to allow controlled DMA or polled operation.

Loop-back

The Engineering kit includes reference software, utilizing external loop-back tests.

The test set-up included PCIBPMC, BA19, SCSI cable, and HDEterm68 to provide the loop-back. The Pin numbers are for the interconnections on the HDEterm68. The IO names can be used to accommodate a different set-up.

Signal	From	To	Signal
MDATA0+	pin 1	pin 12	TDATA0+
MDATA0-	pin 35	pin 46	TDATA0-
MDATA1+	pin 2	pin 13	TDATA1+
MDATA1-	pin 36	pin 47	TDATA1-
MDATA2+	pin 3	pin 14	TDATA2+
MDATA2-	pin 37	pin 48	TDATA2-
MDATA3+	pin 4	pin 15	TDATA3+
MDATA3-	pin 38	pin 49	TDATA3-
MDATA4+	pin 5	pin 16	TDATA4+
MDATA4-	pin 39	pin 50	TDATA4-
MDATA5+	pin 6	pin 17	TDATA5+
MDATA5-	pin 40	pin 51	TDATA5-
MDATA6+	pin 7	pin 18	TDATA6+
MDATA6-	pin 41	pin 52	TDATA6-
MDATA7+	pin 8	pin 19	TDATA7+
MDATA7-	pin 42	pin 53	TDATA7-
MREADY+	pin 9	pin 20	TREADY+
MREADY-	pin 43	pin 54	TREADY-
MSYNC+	pin 10	pin 21	TSYNC+
MSYNC-	pin 44	pin 55	TSYNC-
MCLK+	pin 11	pin 22	TCLK+
MCLK-	pin 45	pin 56	TCLK-

PMC Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BiSerial-III. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

-12V		1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND -		11	12
CLK	GND	13	14
GND -		15	16
	+5V	17	18
	AD31	19	20
AD28-	AD27	21	22
AD25-	GND	23	24
GND -	C/BE3#	25	26
AD22-	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#-	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12-	AD11	47	48
AD9-	+5V	49	50
GND -	C/BE0#	51	52
AD6-	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2-	AD1	59	60
	+5V	61	62
GND		63	64

Figure 22 PMC-BISERIAL-III Pn1 Interface

PMC Module Logic Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BiSerial-III. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
		3	4
	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

Figure 23 PMC-BISERIAL-III Pn2 Interface

PMC Module Front Panel IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC-BiSerial-III. Installed for –FP and –FRP models. Also see the User Manual for your carrier board for more information. Standard BA19 is –FP [no Pn4]

IO_0p (MDATA0+)	IO_0m (MDATA0-)	1	35
IO_1p (MDATA1+)	IO_1m (MDATA1-)	2	36
IO_2p (MDATA2+)	IO_2m (MDATA2-)	3	37
IO_3p (MDATA3+)	IO_3m (MDATA3-)	4	38
IO_4p (MDATA4+)	IO_4m (MDATA4-)	5	39
IO_5p (MDATA5+)	IO_5m (MDATA5-)	6	40
IO_6p (MDATA6+)	IO_6m (MDATA6-)	7	41
IO_7p (MDATA7+)	IO_7m (MDATA7-)	8	42
IO_8p (MREADY+)	IO_8m (MREADY-)	9	43
IO_9p (MSYNC+)	IO_9m (MSYNC-)	10	44
IO_10p (MCLK+)	IO_10m (MCLK-)	11	45
IO_11p (TDATA0+)	IO_11m (TDATA0-)	12	46
IO_12p (TDATA1+)	IO_12m (TDATA1-)	13	47
IO_13p (TDATA2+)	IO_13m (TDATA2-)	14	48
IO_14p (TDATA3+)	IO_14m (TDATA3-)	15	49
IO_15p (TDATA4+)	IO_15m (TDATA4-)	16	50
IO_16p (TDATA5+)	IO_16m (TDATA5-)	17	51
IO_17p (TDATA6+)	IO_17m (TDATA6-)	18	52
IO_18p (TDATA7+)	IO_18m (TDATA7-)	19	53
IO_19p (TREADY+)	IO_19m (TREADY-)	20	54
IO_20p (TSYNC+)	IO_20m (TSYNC-)	21	55
IO_21p (TCLK+)	IO_21m (TCLK-)	22	56
IO_22p ()	IO_22m ()	23	57
IO_23p ()	IO_23m ()	24	58
IO_24p ()	IO_24m ()	25	59
IO_25p ()	IO_25m ()	26	60
IO_26p ()	IO_26m ()	27	61
IO_27p ()	IO_27m ()	28	62
IO_28p ()	IO_28m ()	29	63
IO_29p ()	IO_29m ()	30	64
IO_30p ()	IO_30m ()	31	65
IO_31p ()	IO_31m ()	32	66
IO_32p ()	IO_32m ()	33	67
IO_33p ()	IO_33m ()	34	68

Figure 24 PMC-BISERIAL-III FRONT PANEL Interface

Applications Guide

Interfacing

The pin-out tables are displayed with the pins in the same relative order as the actual connectors. Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power-consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Differential interface devices provide some immunity from, and allow operation when part of the circuit is powered on and part is not. It is better to avoid the issue of going past the safe operating areas by powering the equipment together and by having a good ground reference.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. In addition series resistors are used and can be specified to be something other than the 0 ohm standard value. The connector is pinned out for a standard SCSI II/III cable to be used. It is suggested that this standard cable be used for most of the cable run or an equivalent with proper twisted pairs and shielding.

Terminal Block. We offer a high quality 68 screw terminal block that directly connects to the SCSI II/III cable. The terminal block can mount on standard DIN rails. HDEterm68 [http://www.dyneng.com/HDEterm68.html]

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, or by applying voltage outside of the particular device's rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BiSerial-III is constructed out of 0.062 inch thick high temperature ROHS compliant material.

The traces are matched length from the FPGA ball to the IO pin. The options for front panel and rear panel are isolated with series resistor packs to eliminate bus stubs when one of the connectors is not in use.

Surface mounted components are used.

The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with the connectors and front panel. If more security against vibration is required the stand-offs can be secured against the carrier.

The PMC Module provides a low temperature coefficient of 2.17 W/^{o}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-^{o}C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-BISERIAL-III design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading; forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options. http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $125. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois St. Suite C
Santa Cruz, CA 95060
831-457-8891
831-457-4793 fax
support@dyneng.com

Specifications

Logic Interface:	PMC Logic Interface [PCI] 32/33
Digital Parallel IO:	LVDS IO with BA19 protocol
CLK rates supported:	PLLA is programmed to select Master Clock rate. Approximately 2 MHz is standard interface rate.
Software Interface:	Control Registers, IO registers, IO Read-Back registers, FIFO. R/W, 32 bit boundaries.
Initialization:	Programming procedure documented in this manual
Access Modes:	LW to registers, read-write to most registers
Access Time:	Frame to TRDY 121 nS [4 PCI clocks] or burst mode DMA – 1 word per PCI clock transferred.
Interrupt:	Each port has independently programmable interrupt sources, DMA interrupts included.
Onboard Options:	All Options are Software Programmable
Interface Options:	68 Pin SCSI III connector at front bezel. Rear IO by special request.
Dimensions:	Standard Single PMC Module.
Construction:	Multi-Layer Printed Circuit, Through Hole and Surface Mount Components.
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	TBD mA @ 5V

Order Information

standard temperature range Industrial
PMC-BiSerial-III-BA19 PMC Module with 22 IO channels. One Master and one Target port implemented.
http://www.dyneng.com/pmc_biserial_III.html

Order Options:

Pick One
–FP for front panel IO only [default if no selection made]
-RP for rear panel IO PN4 only
-FRP for both IO connections
Shown for reference. BA19 selection determines [-FP]

Pick any combination to go with IO
-CC to add conformal coating
-ET to change to industrial Temp [-40 - +85C] Standard this design
-COM to change to commercial temp parts [0-70]
-TS to add thumbscrew option – standard is latch block at SCSI connector

Related:
PCIBPMC: PCI to PMC adapter to allow installation of PMC-BiSerial-III into a PCI system.
http://www.dyneng.com/pciBpmc.html

PCIeBPMCX1: PCIe to PMC adapter to allow installation of PMC-BiSerial-III into a PCIe system.
http://www.dyneng.com/pciebpmcx1.html

HDEterm68: 68 position terminal block with two SCSI II/III connectors. PMC-BiSerial-III compatible.
http://www.dyneng.com/HDEterm68.html

HDEcabl68: SCSI II/III cable compatible with FPIO on PMC Parallel IO.
http://www.dyneng.com/HDEcabl68.html

PMC BiSerial III Eng Kit : HDEterm68-MP, HDEcabl68, Windows Driver software, reference schematics. Recommended for first time purchases.
http://www.dyneng.com/pmc_parallel_TTL.html