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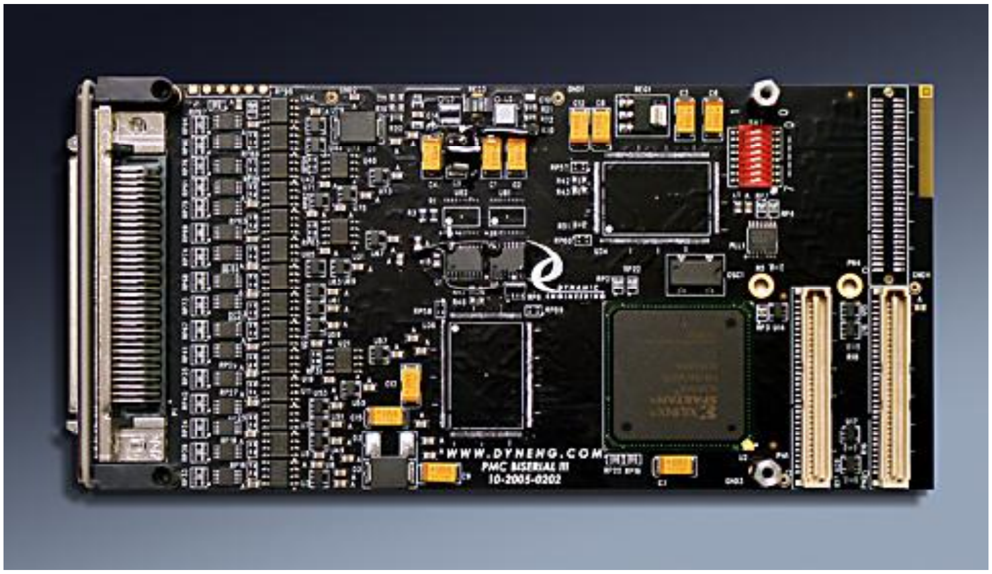
User Manual

PMC-BISERIAL-III BAE9

Eight-Channel UART Interface PMC Module



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PMC-BiSerial-III BAE9
Eight-Channel
PMC Based UART Interface

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Connection of incompatible hardware is likely to cause serious damage.

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Product Description

The PMC-BiSerial-III BAE9 is part of the PMC Module family of modular I/O products by Dynamic Engineering. It meets the PMC and CMC draft Standards. In standard configuration, the PMC-BiSerial-III BAE9 is a Type 1 mechanical with only low profile passive components on the back of the board, one slot wide, with 10 mm inter-board height. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and basic logic design.

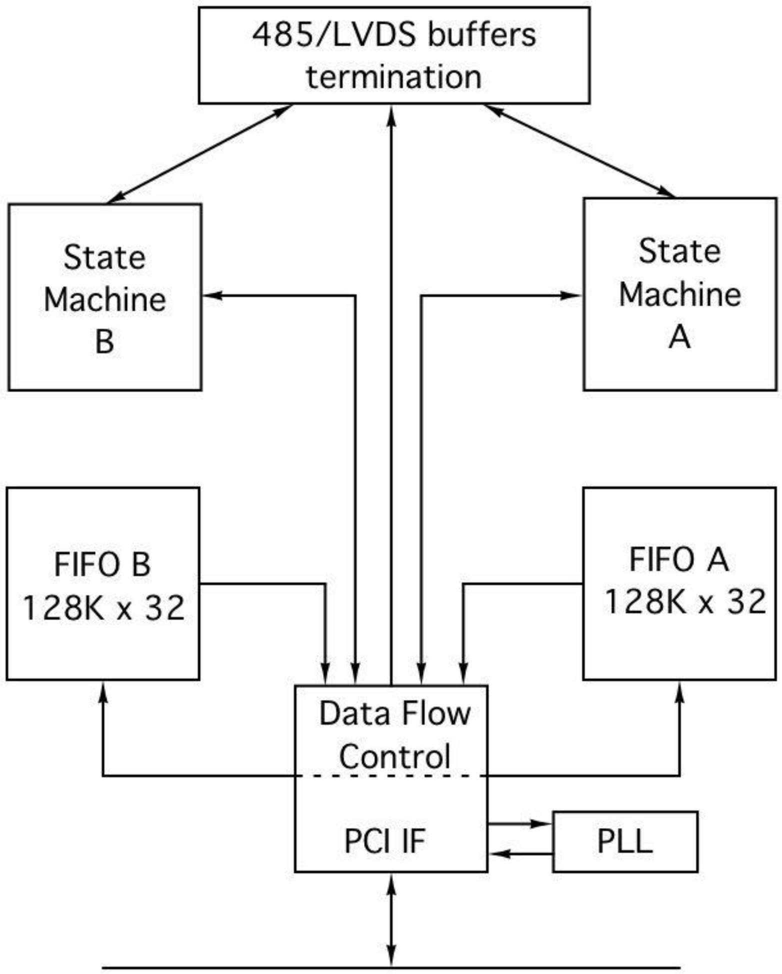


FIGURE 1 PMC-BISERIAL-III BLOCK DIAGRAM

The PMC-BiSerial-III is capable of providing multiple serial protocols using either LVDS or RS-485 I/O standards. The PMC-BiSerial-III standard configuration shown in Figure 1 has two optional data FIFOs that can be as large as 128k x 32 bits to accommodate designs requiring a large amount of buffering. In most designs these FIFOs are not installed and internal FIFOs or dual-port RAMs implemented with the block RAM in the Xilinx FPGA are used instead.

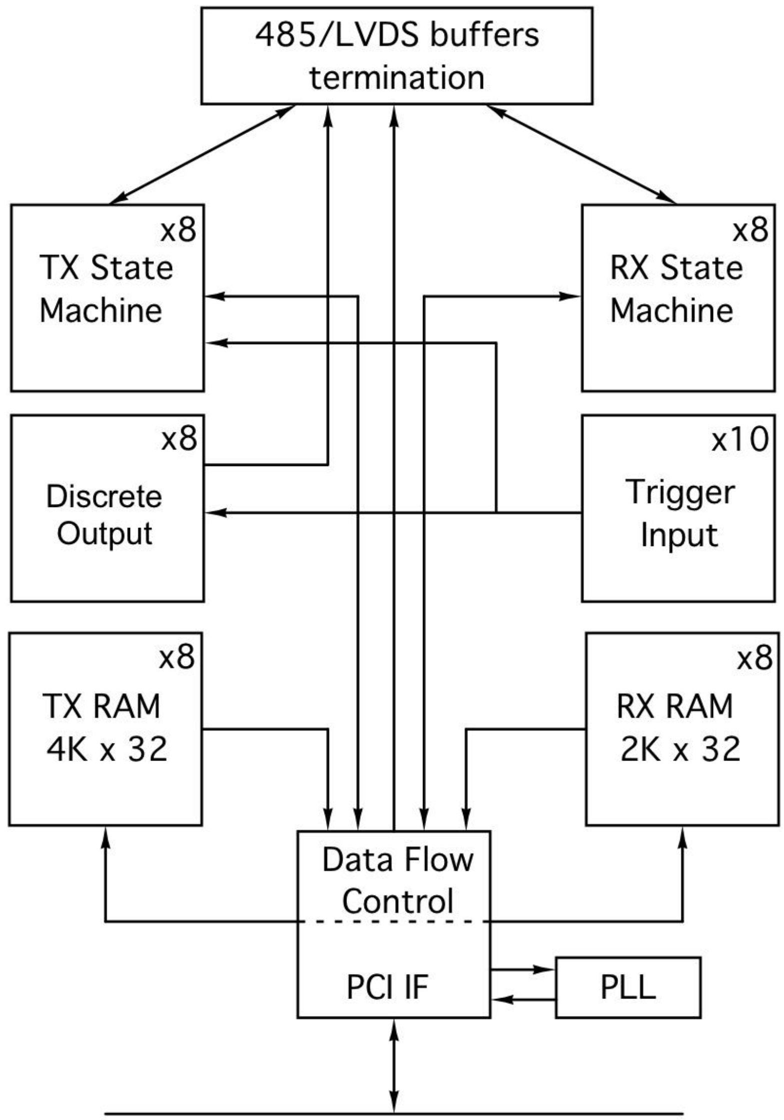


FIGURE 2 PMC-BISERIAL-III BAE9 BLOCK DIAGRAM

The PMC-BiSerial-III BAE9 configuration is shown in figure 2. The protocol implemented provides eight I/O channels each with two RS-485 transceivers. The on-board PLL is used to generate two clocks. PLL clock A supplies the clock reference for the asynchronous message interfaces. PLL clock B supplies the clock reference for the discrete output signal and the discrete input trigger signal monitoring functions. The PLL is programmable and uses a 40 MHz reference oscillator to generate a wide range of frequencies. The UART interface can operate at up to 10 M bits/second using a 160 MHz reference clock.

Data for all channels is sent and received LSB first using a low start-bit and one or two high stop-bits to separate data bytes. An optional parity bit following the eight data bits can be configured to implement odd, even, mark (always high), or space (always low) parity. The marking (idle) state of the interface is high. Transmit and receive messages always start on a 32-bit word boundary. Unsent bytes in a 32-bit transmit word are ignored and unpopulated bytes in the last 32-bit received word are filled with zeros.

Each channel can be configured for either half or full-duplex operation. In half-duplex mode, the receiver data is read from the transmit I/O while the transmitter is in a high impedance state. Pull-up / pull-down resistor packs can be installed on the eight transmit I/O lines to suppress glitching when switching directions in half-duplex mode.

Each channel of the BAE9 implementation has a 16 Mbyte RAM for storing message data for the transmit function and an 8 Mbyte RAM for storing received message data. Each RAM's address space is mapped to the PCI bus Base Address Register 1 (BAR1) to allow write and read access to / from individual 32-bit words. In addition, write DMA access to the transmit RAM and read DMA access from the receive RAM is used to move larger data blocks. The starting address offsets for the transmitter and receiver I/O functions are programmable.

The transmitter state-machine reads data-words sequentially from the transmit RAM starting at the stored starting address offset and sends the data LSB first until the byte-count specified is reached. If the transmitter is re-enabled, it will send data starting at that same starting address offset. In order to send different message data, the starting address must be updated or the RAM data re-written. Multiple messages can be initially stored in the transmit RAM and then independently selected by the user by changing the starting address offset for the transmitter.

The receiver state-machine will begin storing received data-words in the next word after the programmed starting address offset. When the message is complete, a status-word which contains the message byte-count and the starting address of the next message will be written to the initial RAM location that was skipped when the message data was written. Unlike the transmitter, the receiver will store subsequent messages in the memory space immediately following the message just received. By reading the status-word of the first message, the address of the status-word for the next message is known. This process can be continued until the address of the message of interest is found. Using the byte count in that message's status-word, a DMA can be setup to quickly read the message data and process accordingly.

Various interrupts are supported by the PMC-BiSerial-III BAE9. An interrupt can be configured to occur at the end of a received or transmitted message. Receiver parity or framing errors are detected and latched, and can also be configured to cause an interrupt. All interrupts can be individually masked, and a master channel interrupt enable is also provided to disable all interrupts for a channel. The current status of interrupt conditions is available even when the interrupt is disabled making it possible to operate in a polled mode. Most configuration registers support read and write operations for maximum software convenience. All addresses are long word (32-bit) aligned.

Potentially thirty-four differential I/O are available at the front bezel for the serial signals. The drivers and receivers conform to the RS-485 specification. The RS-485 signals are selectively terminated with 100Ω by software. The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. Optional pull-up/pull-down resistor packs can also be installed to provide a logic '1' on undriven lines. In this design 4.7 kΩ pull-up/pull-down resistors have been installed on the eight transmit lines to prevent erroneous data when switching directions in half-duplex mode.

The PMC-BiSerial-III BAE9 design uses all 34 I/O lines. Sixteen for the UARTs (one in and one out for each of the eight channels), eight for the discrete output signals (one per channel) and ten discrete input signals any one of which can be selected on a per channel basis.

Other custom interfaces are available on request. We will redesign the state machines and create a custom interface protocol that meets your requirements. That protocol will then be offered as a "standard" special order product. Please see our web page for current protocols offered. If none of these fulfill your needs, contact Dynamic Engineering with your custom application.

Since the PMC-BiSerial-III BAE9 conforms to the PMC and CMC draft standards, it is guaranteed to be compatibile with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

The PMC-BiSerial-III BAE9 uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with the PMC-BiSerial-III BAE9, please let us know. We may be able to do a special build with a different height connector to compensate.

Theory of Operation

The PMC-BiSerial-III BAE9 features an XC3S4000-5 Spartan 3 Xilinx FPGA. The FPGA contains all of the registers, dual-port RAMs and protocol controlling elements of the PMC-BiSerial-III BAE9 design. Only the transceivers, switches and PLL circuit are external to the Xilinx device.

A logic block within the Xilinx controls the PCI interface to the host CPU. The PMC-BiSerial-III BAE9 requires one wait state for read / write cycles to any address. The wait states refer to the number of clocks after the PCI core decodes the address and control signals and before the "terminate with data" state is reached. Two additional clock periods account for the delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather DMA is supported in this design with the memory page information stored in host RAM as a series of chaining descriptors. Once the physical address of the first chaining descriptor is written to the appropriate DMA pointer register, the interface will read a 16-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the I/O buffer passed to the read or write call. The next four bytes specify the address offset in the corresponding local RAM that is the target of the data transfer. The next four bytes represent a long-word indicating the length of the data-block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to a '1' if this descriptor is the last in the chain. Bit one is set to a '1' if the I/O transfer is from the PMC-BiSerial-III BAE9 board to host memory, and a '0' if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one.

Transmitting data requires a number of steps to be performed. The PLL must be programmed to supply the I/O clock. The message data must be written to the TX RAM, the starting address of the message stored and the transmitter configuration specified. Finally, the transmitter must be enabled along with the number of bytes to be sent. These steps do not need to be performed in this order, but they must all be done to accomplish the transfer. The least significant byte of the RAM word is sent first then the next significant byte follows until the entire 32-bit word is sent. If a byte count is requested that is not divisible by four, the remaining bytes of the last RAM word are discarded and a subsequent transmission will begin with a new 32-bit word. The transmitter can operate in one of four modes: triggered, where the transmitter waits for a trigger signal to be seen then waits for a programmable delay count to expire before sending the requested message; periodic, where the message is sent immediately and thereafter once for each time a programmable period count is reached; one-shot, where the message is sent immediately only once; and triggered periodic, which initially behaves like the triggered mode, but then repeats the message like the periodic mode. Multiple messages can be pre-written to the transmit RAM and then randomly selected by the user by rewriting the starting I/O address.

In order to receive data it is only necessary to configure the PLL, configure and enable the receiver and wait for data to be received. A 16-bit counter is incremented for each data byte received. Once the reception has started, a 32-bit data word will be stored in the receive RAM for each four bytes received. The first byte is stored in the least significant byte of the RAM word and each subsequent byte is stored in the next most significant byte. When the input data line is idle for at least eight bit-periods the reception will terminate. This will cause the received byte count to be written to the byte count register, the message status-word to be written to RAM at the beginning of the message memory space and the receiver done status bit set. If the last RAM word was not completely filled, the last partial word will be written to the receive RAM with the unfilled bytes set to zeros. If the receiver start clear enable is set, the receiver enable bit will be cleared, otherwise the receiver will remain enabled and will wait for the next start-bit to continue receiving data.

Each channel also has a discrete output signal that can be configured to operate in the same four modes as the transmit UART. The signal is a pulse that is determined by the programmable period and duty counts. PLL clock B supplies the timing reference for these counts. The polarity of the signal output and the trigger input, as well as the trigger input for the transmit UART, can be selected by control bits in the transmit control register.

Additionally there are ten RS-485 I/O lines used for discrete input signals used as triggers by the transmit UART or discrete output signals. Each channel can select one of these ten lines without restriction (any or all channels can select the same line). A trigger monitor function counts the duration of the trigger high and low logic levels. Four latched status bits are set if the high or low logic levels exceed minimum or maximum programmable time counts. The counts of the last high and low level pulse are stored and are available to be read. In rev. D these count fields were expanded from sixteen to twenty-two bits and in rev E the ability to detect a steady-state signal was added. PLL clock B is used as a timing reference for these functions.

The baud-rate of the UART interface can be programmed to one of 48 values without changing the PLL clock A frequency. These values represent a four-to-one ratio and each channel's baud-rate can be adjusted independently. Typically, the receive UART uses a 16x clock to decode the asynchronous data-stream since the sender and receiver may be operating at slightly different clock rates. To allow the receiver to operate over a wider frequency range, we divide the bit period into three sections. During the beginning section, if a data transition is seen, the bit-time counter will reset as it assumes this is the beginning of a new data-bit. The middle of the middle section is where the data value is sampled and the shift-register advanced. The end section will again be looking for a data transition, and if seen will reset the bit-time counter and move to the beginning section of the next bit. The count values that mark the limits of these three sections are modified based on the clocks per bit-period setting which is programmable from 16 to 64 clocks per bit.

The values of the transition counts for each bit-width value and the resulting baud-rates (based on a PLL clock A frequency of 160 MHz) are listed below.

Register	Divide	Baud Rate	low	mid	high	end
0x0F	16	10.000 Mbps	2	7	13	15
0x10	17	9.412 Mbps	3	8	13	16
0x11	18	8.889 Mbps	3	8	14	17
0x12	19	8.421 Mbps	3	9	15	18
0x13	20	8.000 Mbps	3	9	16	19
0x14	21	7.619 Mbps	3	10	17	20
0x15	22	7.273 Mbps	3	10	18	21
0x16	23	6.957 Mbps	3	11	19	22
0x17	24	6.667 Mbps	3	11	20	23
0x18	25	6.400 Mbps	4	12	20	24
0x19	26	6.154 Mbps	4	12	21	25
0x1A	27	5.926 Mbps	4	13	22	26
0x1B	28	5.714 Mbps	4	13	23	27
0x1C	29	5.517 Mbps	4	14	24	28
0x1D	30	5.333 Mbps	4	14	25	29
0x1E	31	5.161 Mbps	4	15	26	30
0x1F	32	5.000 Mbps	4	15	27	31
0x20	33	4.848 Mbps	5	16	27	32
0x21	34	4.706 Mbps	5	16	28	33
0x22	35	4.571 Mbps	5	17	29	34
0x23	36	4.444 Mbps	5	17	30	35
0x24	37	4.324 Mbps	5	18	31	36
0x25	38	4.211 Mbps	5	18	32	37
0x26	39	4.103 Mbps	5	19	33	38
0x27	40	4.000 Mbps	5	19	34	39
0x28	41	3.902 Mbps	6	20	34	40
0x29	42	3.810 Mbps	6	20	35	41
0x2A	43	3.721 Mbps	6	21	36	42
0x2B	44	3.636 Mbps	6	21	37	43
0x2C	45	3.556 Mbps	6	22	38	44
0x2D	46	3.478 Mbps	6	22	39	45
0x2E	47	3.404 Mbps	6	23	40	46
0x2F	48	3.333 Mbps	6	23	41	47
0x30	49	3.265 Mbps	7	24	41	48
0x31	50	3.200 Mbps	7	24	42	49
0x32	51	3.137 Mbps	7	25	43	50
0x33	52	3.077 Mbps	7	25	44	51
0x34	53	3.019 Mbps	7	26	45	52
0x35	54	2.963 Mbps	7	26	46	53
0x36	55	2.909 Mbps	7	27	47	54
0x37	56	2.857 Mbps	7	27	48	55
0x38	57	2.807 Mbps	8	28	48	56
0x39	58	2.759 Mbps	8	28	49	57
0x3A	59	2.712 Mbps	8	29	50	58
0x3B	60	2.667 Mbps	8	29	51	59
0x3C	61	2.623 Mbps	8	30	52	60
0x3D	62	2.581 Mbps	8	30	53	61
0x3E	63	2.540 Mbps	8	31	54	62
0x3F	64	2.500 Mbps	8	31	55	63

Programming

Programming the PMC-BiSerial-III BAE9 requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BiSerial-III BAE9 "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

Before I/O data can be sent or received, the PLL must be programmed to the desired clock configuration. The PLL is connected to the Xilinx by an I^2C serial bus. The PLL internal registers are loaded with 40 bytes of data that are derived from a .jed file generated by the CyberClock utility from Cypress semiconductor http://www.dyneng.com/CyberClocks.zip. Routines to program the PLL are included in the driver and UserApp code provided in the engineering kit for the board.

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the TX/RX interrupts. After an interrupt is received, new TX data can be written or RX data retrieved. An efficient loop can then be implemented to process the data. New messages can be setup even as the current one is in progress.

If more than one interrupt is enabled, then the software needs to read the status to see which source caused the interrupt. The status bits are latched, and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status register and write that value back to clear all the latched interrupt status bits before starting a transfer. This will insure that the interrupt status values read by the interrupt service routine came from the current transfer.

If DMA is to be used it will be necessary to acquire blocks of non-paged memory that are accessible from the PCI bus in which to store the DMA chaining descriptor list entries.

Refer to the Theory of Operation section above and the register definition section below for more information regarding the exact sequencing and interrupt definitions.

The PMC-BiSerial-III BAE9 VendorId = 0xDCBA. The CardId = 0x0048. The device class code is 0x0680 (PCI bridge – other)

Address Map (BAR 0)

Register Name	Offset	Description
BAE9_BASE_CONTROL	0x0000	Base Control Register
BAE9_PLL_WRITE	0x0000	Base Control - Bits 16-19 Used for PLL Control
BAE9_PLL_READ	0x0004	Switch Port Bit 19 Used for pll_sdat Input
BAE9_USER_SWITCH	0x0004	User Switch Read Port and Xilinx Design Revision
BAE9_CHAN_0_CONTROL	0x0010	Channel 0 Control Register
BAE9_CHAN_0_STATUS	0x0014	Channel 0 Status Register
BAE9_CHAN_0_WR_DMA_PNTR	0x0018	Channel 0 Write DMA Physical PCI dpr Address
BAE9_CHAN_0_TX_ADDRESS	0x0018	Channel 0 Write DMA Address Offsets (read only)
BAE9_CHAN_0_RD_DMA_PNTR	0x001C	Channel 0 Read DMA Physical PCI dpr Address
BAE9_CHAN_0_RX_ADDRESS	0x001C	Channel 0 Read DMA Address Offsets (read only)
BAE9_CHAN_0_IO_ADDR_LAT	0x0020	Channel 0 Latch starting addresses for TX and RX I/O
BAE9_CHAN_0_TRIG_CNT_LAT	0x0024	Channel 0 Latch Limit Counts for Trigger Signal Input
BAE9_CHAN_0_DSCRT_OUT_LAT	0x0028	Channel 0 Latch Timing Counts for Discrete Output Signal
BAE9_CHAN_0_TX_CONTROL	0x002C	Channel 0 TX Control Register
BAE9_CHAN_0_RX_CONTROL	0x0030	Channel 0 RX Control Register
BAE9_CHAN_0_TX_UART_LAT	0x0034	Channel 0 Latch Timing Counts for UART Output
BAE9_CHAN_0_TX_START	0x0038	Channel 0 TX Start Latch and Byte Count
BAE9_CHAN_0_RX_START	0x003C	Channel RX Start Latch (write) / RX Byte Count (read)
BAE9_CHAN_1_CONTROL	0x0040	Channel 1 Control Register
BAE9_CHAN_1_STATUS	0x0044	Channel 1 Status Register
BAE9_CHAN_1_WR_DMA_PNTR	0x0048	Channel 1 Write DMA Physical PCI dpr Address
BAE9_CHAN_1_TX_ADDRESS	0x0048	Channel 1 Write DMA Address Offsets (read only)
BAE9_CHAN_1_RD_DMA_PNTR	0x004C	Channel 1 Read DMA Physical PCI dpr Address
BAE9_CHAN_1_RX_ADDRESS	0x004C	Channel 1 Read DMA Address Offsets (read only)
BAE9_CHAN_1_IO_ADDR_LAT	0x0050	Channel 1 Latch starting addresses for TX and RX I/O
BAE9_CHAN_1_TRIG_CNT_LAT	0x0054	Channel 1 Latch Limit Counts for Trigger Signal Input
BAE9_CHAN_1_DSCRT_OUT_LAT	0x0058	Channel 1 Latch Timing Counts for Discrete Output Signal
BAE9_CHAN_1_TX_CONTROL	0x005C	Channel 1 TX Control Register
BAE9_CHAN_1_RX_CONTROL	0x0060	Channel 1 RX Control Register
BAE9_CHAN_1_TX_UART_LAT	0x0064	Channel 1 Latch Timing Counts for UART Output
BAE9_CHAN_1_TX_START	0x0068	Channel 1 TX Start Latch and Byte Count
BAE9_CHAN_1_RX_START	0x006C	Channel 1 RX Start Latch (write) / RX Byte Count (read)
BAE9_CHAN_2_CONTROL	0x0070	Channel 2 Control Register
BAE9_CHAN_2_STATUS	0x0074	Channel 2 Status Register
BAE9_CHAN_2_WR_DMA_PNTR	0x0078	Channel 2 Write DMA Physical PCI dpr Address
BAE9_CHAN_2_TX_ADDRESS	0x0078	Channel 2 Write DMA Address Offsets (read only)
BAE9_CHAN_2_RD_DMA_PNTR	0x007C	Channel 2 Read DMA Physical PCI dpr Address
BAE9_CHAN_2_RX_ADDRESS	0x007C	Channel 2 Read DMA Address Offsets (read only)
BAE9_CHAN_2_IO_ADDR_LAT	0x0080	Channel 2 Latch starting addresses for TX and RX I/O
BAE9_CHAN_2_TRIG_CNT_LAT	0x0084	Channel 2 Latch Limit Counts for Trigger Signal Input
BAE9_CHAN_2_DSCRT_OUT_LAT	0x0088	Channel 2 Latch Timing Counts for Discrete Output Signal
BAE9_CHAN_2_TX_CONTROL	0x008C	Channel 2 TX Control Register
BAE9_CHAN_2_RX_CONTROL	0x0090	Channel 2 RX Control Register
BAE9_CHAN_2_TX_UART_LAT	0x0094	Channel 2 Latch Timing Counts for UART Output
BAE9_CHAN_2_TX_START	0x0098	Channel 2 TX Start Latch and Byte Count
BAE9_CHAN_2_RX_START	0x009C	Channel 2 RX Start Latch (write) / RX Byte Count (read)
BAE9_CHAN_3_CONTROL	0x00A0	Channel 3 Control Register
BAE9_CHAN_3_STATUS	0x00A4	Channel 3 Status Register
BAE9_CHAN_3_WR_DMA_PNTR	0x00A8	Channel 3 Write DMA Physical PCI dpr Address
BAE9_CHAN_3_TX_ADDRESS	0x00A8	Channel 3 Write DMA Address Offsets (read only)
BAE9_CHAN_3_RD_DMA_PNTR	0x00AC	Channel 3 Read DMA Physical PCI dpr Address
BAE9_CHAN_3_RX_ADDRESS	0x00AC	Channel 3 Read DMA Address Offsets (read only)
BAE9_CHAN_3_IO_ADDR_LAT	0x00B0	Channel 3 Latch starting addresses for TX and RX I/O
BAE9_CHAN_3_TRIG_CNT_LAT	0x00B4	Channel 3 Latch Limit Counts for Trigger Signal Input
BAE9_CHAN_3_DSCRT_OUT_LAT	0x00B8	Channel 3 Latch Timing Counts for Discrete Output Signal
BAE9_CHAN_3_TX_CONTROL	0x00BC	Channel 3 TX Control Register
BAE9_CHAN_3_RX_CONTROL	0x00C0	Channel 3 RX Control Register
BAE9_CHAN_3_TX_UART_LAT	0x00C4	Channel 3 Latch Timing Counts for UART Output
BAE9_CHAN_3_TX_START	0x00C8	Channel 3 TX Start Latch and Byte Count
BAE9_CHAN_3_RX_START	0x00CC	Channel 3 RX Start Latch (write) / RX Byte Count (read)

FIGURE 3 PMC-BISERIAL-III BAE9 REGISTER ADDRESS MAP

BAE9_CHAN_4_CONTROL	0x00D0	Channel 4 Control Register
BAE9_CHAN_4_STATUS	0x00D4	Channel 4 Status Register
BAE9_CHAN_4_WR_DMA_PNTR	0x00D8	Channel 4 Write DMA Physical PCI dpr Address
BAE9_CHAN_4_TX_ADDRESS	0x00D8	Channel 4 Write DMA Address Offsets (read only)
BAE9_CHAN_4_RD_DMA_PNTR	0x00DC	Channel 4 Read DMA Physical PCI dpr Address
BAE9_CHAN_4_RX_ADDRESS	0x00DC	Channel 4 Read DMA Address Offsets (read only)
BAE9_CHAN_4_IO_ADDR_LAT	0x00E0	Channel 4 Latch starting addresses for TX and RX I/O
BAE9_CHAN_4_TRIG_CNT_LAT	0x00E4	Channel 4 Latch Limit Counts for Trigger Signal Input
BAE9_CHAN_4_DSCRT_OUT_LAT	0x00E8	Channel 4 Latch Timing Counts for Discrete Output Signal
BAE9_CHAN_4_TX_CONTROL	0x00EC	Channel 4 TX Control Register
BAE9_CHAN_4_RX_CONTROL	0x00F0	Channel 4 RX Control Register
BAE9_CHAN_4_TX_UART_LAT	0x00F4	Channel 4 Latch Timing Counts for UART Output
BAE9_CHAN_4_TX_START	0x00F8	Channel 4 TX Start Latch and Byte Count
BAE9_CHAN_4_RX_START	0x00FC	Channel 4 RX Start Latch (write) / RX Byte Count (read)
BAE9_CHAN_5_CONTROL	0x0100	Channel 5 Control Register
BAE9_CHAN_5_STATUS	0x0104	Channel 5 Status Register
BAE9_CHAN_5_WR_DMA_PNTR	0x0108	Channel 5 Write DMA Physical PCI dpr Address
BAE9_CHAN_5_TX_ADDRESS	0x0108	Channel 5 Write DMA Address Offsets (read only)
BAE9_CHAN_5_RD_DMA_PNTR	0x010C	Channel 5 Read DMA Physical PCI dpr Address
BAE9_CHAN_5_RX_ADDRESS	0x010C	Channel 5 Read DMA Address Offsets (read only)
BAE9_CHAN_5_IO_ADDR_LAT	0x0110	Channel 5 Latch starting addresses for TX and RX I/O
BAE9_CHAN_5_TRIG_CNT_LAT	0x0114	Channel 5 Latch Limit Counts for Trigger Signal Input
BAE9_CHAN_5_DSCRT_OUT_LAT	0x0118	Channel 5 Latch Timing Counts for Discrete Output Signal
BAE9_CHAN_5_TX_CONTROL	0x011C	Channel 5 TX Control Register
BAE9_CHAN_5_RX_CONTROL	0x0120	Channel 5 RX Control Register
BAE9_CHAN_5_TX_UART_LAT	0x0124	Channel 5 Latch Timing Counts for UART Output
BAE9_CHAN_5_TX_START	0x0128	Channel 5 TX Start Latch and Byte Count
BAE9_CHAN_5_RX_START	0x012C	Channel 5 RX Start Latch (write) / RX Byte Count (read)
BAE9_CHAN_6_CONTROL	0x0130	Channel 6 Control Register
BAE9_CHAN_6_STATUS	0x0134	Channel 6 Status Register
BAE9_CHAN_6_WR_DMA_PNTR	0x0138	Channel 6 Write DMA Physical PCI dpr Address
BAE9_CHAN_6_TX_ADDRESS	0x0138	Channel 6 Write DMA Address Offsets (read only)
BAE9_CHAN_6_RD_DMA_PNTR	0x013C	Channel 6 Read DMA Physical PCI dpr Address
BAE9_CHAN_6_RX_ADDRESS	0x013C	Channel 6 Read DMA Address Offsets (read only)
BAE9_CHAN_6_IO_ADDR_LAT	0x0140	Channel 6 Latch starting addresses for TX and RX I/O
BAE9_CHAN_6_TRIG_CNT_LAT	0x0144	Channel 6 Latch Limit Counts for Trigger Signal Input
BAE9_CHAN_6_DSCRT_OUT_LAT	0x0148	Channel 6 Latch Timing Counts for Discrete Output Signal
BAE9_CHAN_6_TX_CONTROL	0x014C	Channel 6 TX Control Register
BAE9_CHAN_6_RX_CONTROL	0x0150	Channel 6 RX Control Register
BAE9_CHAN_6_TX_UART_LAT	0x0154	Channel 6 Latch Timing Counts for UART Output
BAE9_CHAN_6_TX_START	0x0158	Channel 6 TX Start Latch and Byte Count
BAE9_CHAN_6_RX_START	0x015C	Channel 6 RX Start Latch (write) / RX Byte Count (read)
BAE9_CHAN_7_CONTROL	0x0160	Channel 7 Control Register
BAE9_CHAN_7_STATUS	0x0164	Channel 7 Status Register
BAE9_CHAN_7_WR_DMA_PNTR	0x0168	Channel 7 Write DMA Physical PCI dpr Address
BAE9_CHAN_7_TX_ADDRESS	0x0168	Channel 7 Write DMA Address Offsets (read only)
BAE9_CHAN_7_RD_DMA_PNTR	0x016C	Channel 7 Read DMA Physical PCI dpr Address
BAE9_CHAN_7_RX_ADDRESS	0x016C	Channel 7 Read DMA Address Offsets (read only)
BAE9_CHAN_7_IO_ADDR_LAT	0x0170	Channel 7 Latch starting addresses for TX and RX I/O
BAE9_CHAN_7_TRIG_CNT_LAT	0x0174	Channel 7 Latch Limit Counts for Trigger Signal Input
BAE9_CHAN_7_DSCRT_OUT_LAT	0x0178	Channel 7 Latch Timing Counts for Discrete Output Signal
BAE9_CHAN_7_TX_CONTROL	0x017C	Channel 7 TX Control Register
BAE9_CHAN_7_RX_CONTROL	0x0180	Channel 7 RX Control Register
BAE9_CHAN_7_TX_UART_LAT	0x0184	Channel 7 Latch Timing Counts for UART Output
BAE9_CHAN_7_TX_START	0x0188	Channel 7 TX Start Latch and Byte Count
BAE9_CHAN_7_RX_START	0x018C	Channel 7 RX Start Latch (write) / RX Byte Count (read)

FIGURE 3 PMC-BISERIAL-III BAE9 REGISTER ADDRESS MAP (CONTINUED)

Address Map (BAR 1)

Memory Name	Memory Range	Description
BAE9_CHAN_0_TX_RAM	0x00000-0x03FFC	Channel 0 Transmit RAM
BAE9_CHAN_0_RX_RAM	0x04000-0X05FFC	Channel 0 Receive RAM
BAE9_CHAN_1_TX_RAM	0x08000-0x0BFFC	Channel 1 Transmit RAM
BAE9_CHAN_1_RX_RAM	0x0C000-0X0DFFC	Channel 1 Receive RAM
BAE9_CHAN_2_TX_RAM	0x10000-0x13FFC	Channel 2 Transmit RAM
BAE9_CHAN_2_RX_RAM	0x14000-0X15FFC	Channel 2 Receive RAM
BAE9_CHAN_3_TX_RAM	0x18000-0x1BFFC	Channel 3 Transmit RAM
BAE9_CHAN_3_RX_RAM	0x1C000-0X1DFFC	Channel 3 Receive RAM
BAE9_CHAN_4_TX_RAM	0x20000-0x23FFC	Channel 4 Transmit RAM
BAE9_CHAN_4_RX_RAM	0x24000-0X25FFC	Channel 4 Receive RAM
BAE9_CHAN_5_TX_RAM	0x28000-0x2BFFC	Channel 5 Transmit RAM
BAE9_CHAN_5_RX_RAM	0x2C000-0X2DFFC	Channel 5 Receive RAM
BAE9_CHAN_6_TX_RAM	0x30000-0x33FFC	Channel 6 Transmit RAM
BAE9_CHAN_6_RX_RAM	0x34000-0X35FFC	Channel 6 Receive RAM
BAE9_CHAN_7_TX_RAM	0x38000-0x3BFFC	Channel 7 Transmit RAM
BAE9_CHAN_7_RX_RAM	0x3C000-0X3DFFC	Channel 7 Receive RAM

FIGURE 4 PMC-BISERIAL-III BAE9 MEMORY BLOCK ADDRESS MAP

Register Definitions

BAE9_BASE_CONTROL

[0x0000] Base Control (read/write)

Base Control

Data Bit	Description
31-20	Spare
19	PLL Sdata Output
18	PLL S2 Output
17	PLL Sclk Output
16	PLL Enable
15-10	Spare
9-0	Termination Enables for Discrete Inputs

FIGURE 5 PMC-BISERIAL-III BAE9 BASE CONTROL

All bits are active high and are reset on power-up or reset command, except PLL enable, which defaults to enabled (high) on power-up or reset.

Termination Enables for Discrete Inputs: When one of these bits is set to a one, the corresponding discrete input line termination is enabled. I/O lines 24 – 33 correspond to discrete inputs 0 – 9 respectively.

PLL Enable: When this bit is set to a one, the signals used to program and read the PLL are enabled.

PLL Sclk/Sdata Output: These signals are used to program the PLL over the I^2C serial interface. Sclk is always an output whereas Sdata is bi-directional. This register is where the Sdata output value is specified. When Sdata is an input it is read from the User Switch Port.

PLL S2 Output: This is an additional control line to the PLL that can be used to select additional pre-programmed frequencies.

BAE9_USER_SWITCH

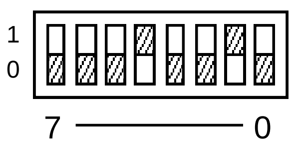
[0x0004] User Switch Port (read only)

Dip-Switch Port

Data Bit	Description
31-24	Channel Interrupt Status
23-20	Spare
19	PLL Sdata Input
18-16	Spare
15-8	Xilinx Design Revision Number
7-0	Switch Setting

FIGURE 6 PMC-BISERIAL-III BAE9 USER SWITCH PORT

Switch Setting: The user switch is read through this port. The bits are read as the lowest byte in the port. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



Xilinx Design Revision Number: The value of the second byte of this port is the rev. number of the Xilinx design (currently 0x05 - rev. E.)

PLL Sdata Input: The PLL_sdata bi-directional line is read using this bit. This line is used to read the register contents of the PLL.

Channel Interrupt Status: These eight bits represent the state of the eight channel interrupts. When a one is read, it indicates that the respective channel's interrupt is active. A zero indicates that the channel's interrupt is not active.

BAE9_CHAN_0-7_CONTROL

[0x0010, 40, 70, A0, D0, 100, 130, 160] Channel Control (read/write)

Channel Control

Data Bit	Description
31-11	Spare
10	Auto Direction Switch Enable
9	Full-Duplex Enable
8	Trigger Monitor Enable
7	Read DMA Interrupt Enable
6	Write DMA Interrupt Enable
5	Force Interrupt
4	Master Interrupt Enable
3-0	Discrete Input Select

FIGURE 7 PMC-BISERIAL-III BAE9 CHANNEL CONTROL

Discrete Input Select: This field selects one of the ten discrete input signals to be used to trigger the UART transmission and/or the discrete output signal. Values from 0 to 9 are accepted. There are no restrictions on which signal can be used and any or all channels can share the same input line.

Master Interrupt Enable: When this bit is set to a one, all enabled interrupts (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one, a system interrupt will occur provided the master interrupt enable is set. This is useful for interrupt testing.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA writes and reads respectively. The DMA interrupts are not affected by the Master Interrupt Enable.

Trigger Monitor Enable: When this bit is set to a one, the trigger monitor function is enabled. This circuit, using PLL clock B for a timing reference, counts the duration of the high and low levels of the selected trigger input signal. There are also four latched status bits that report counts that are above or below programmable counts for each level. When this bit is a zero, the trigger monitor is disabled.

Full-Duplex Enable: When this bit is set to a one, the respective channel I/O will operate in full-duplex mode. This means the transmit and receive data are transferred on separate I/O lines and these transfers can occur simultaneously. When this bit is zero, the I/O will operate in half-duplex mode. This means the transmit and receive data are transferred on the same I/O line (the full-duplex transmit I/O line) and the transfer direction alternates with the transmitter in a high impedance state when the receiver is active.

Auto Direction Switch Enable: When this bit is set to a one, and the channel I/O is operating in half-duplex mode, the I/O interface will automatically change directions when the current message completes provided transmit and receive interfaces are both enabled. When this bit is zero, the I/O interface will not switch directions unless explicitly commanded to do so.

BAE9_CHAN_0-7_STATUS

[0x0014, 44, 74, A4, D4, 104, 134, 164] Channel Status Read/Clear Latch Write

Channel Status

Data Bit	Description
31	Channel Interrupt Active
30-28	Spare
27	User Interrupt Condition Occurred
26-18	Spare
17	Latch Trigger Monitor Counts (write only)
16	Clear Trigger Monitor Counts (write only)
15	Trigger Low-Level Under Limit
14	Trigger Low-Level Over Limit
13	Trigger High-Level Under Limit
12	Trigger High-Level Over Limit
10-11	Spare
9	Read DMA Idle
8	Write DMA Idle
7	Read DMA Interrupt Occurred
6	Write DMA Interrupt Occurred
5	Read DMA Error Occurred
4	Write DMA Error Occurred
3	Receive Framing Error Occurred
2	Receive Parity Error Occurred
1	Receive Done Interrupt Occurred
0	Transmit Done Interrupt Occurred

FIGURE 8 PMC-BISERIAL-III BAE9 CHANNEL STATUS

Transmit Done Interrupt Occurred: When a one is read, it indicates that the transmit state-machine has completed a message. A zero indicates that a transmit message has not been completed. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Done Interrupt Occurred: When a one is read, it indicates that the receive state-machine has received at least one complete message. At least one byte must have been received and then the receive data line must be idle for at least eight bit-periods for a message to be considered completed. A zero indicates that a complete message has not been received. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Parity Error Occurred: When a one is read, it indicates that a parity error was detected in a received data-byte. A zero indicates that no parity error was detected. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Framing Error Occurred: When a one is read, it indicates that a framing error has been detected in the receive data stream. This is caused by an incorrect number or polarity of stop bits. A zero indicates that no framing error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Write/Read DMA Error Occurred: When a one is read, a write or read DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the initial descriptor pointer address or next pointer of one of the chaining descriptors is incorrect. A zero indicates that no write or read DMA error has occurred. These bits are latched and can be cleared by writing back to the Status register with a one in the appropriate bit position.

Write/Read DMA Interrupt Occurred: When a one is read, a write/read DMA interrupt is latched. This indicates that the scatter-gather list for the current write or read DMA has completed, but the associated interrupt has yet to be processed. A zero indicates that no write or read DMA interrupt is pending.

Write/Read DMA Idle: When a one is read, a write/read DMA interrupt is latched. This indicates that the scatter-gather list for the current write or read DMA has completed, but the associated interrupt has yet to be processed. A zero indicates that no write or read DMA interrupt is pending.

Trigger High-Level Over Limit: When a one is read, the duration of the high portion of the trigger input signal has exceeded the appropriate programmed count value. A zero indicates that this condition has not occurred since the latch was last cleared.

Trigger High-Level Under Limit: When a one is read, the duration of the high portion of the trigger input signal was less than the appropriate programmed count value. A zero indicates that this condition has not occurred since the latch was last cleared.

Trigger Low-Level Over Limit: When a one is read, the duration of the low portion of the trigger input signal has exceeded the appropriate programmed count value. A zero indicates that this condition has not occurred since the latch was last cleared.

Trigger Low-Level Under Limit: When a one is read, the duration of the low portion of the trigger input signal was less than the appropriate programmed count value. A zero indicates that this condition has not occurred since the latch was last cleared.

Clear Trigger Monitor Counts: When a one is written to this bit, the trigger monitor time counters that report the duration of the high and low levels of the trigger input signal are stopped and the counts cleared. This is required to prepare for detection of a constant level signal on the trigger input.

Latch Trigger Monitor Counts: When a one is written to this bit, the trigger monitor high and low level time counter values are entered into the latches that report the duration of the respective levels. If these counts are both zero it means that no rising or falling edge has occurred since the counts were cleared. This fact, plus the signal level read from the trigger monitor high or low count register, indicates that a constant level signal of the polarity read is driving the trigger signal input.

User Interrupt Condition Occurred: When a one is read, it indicates that an enabled user interrupt condition has occurred. These conditions include the TX and RX done interrupts as well as the RX parity and framing error interrupts. Also the Force Interrupt bit will cause this bit to be asserted. A system interrupt will occur if the Master Interrupt Enable is set. A zero indicates that no enabled user interrupt condition is active.

Channel Interrupt Active: When a one is read, it indicates that a system interrupt is asserted caused by an enabled channel interrupt condition. A zero indicates that no system interrupt is pending from an enabled channel interrupt condition.

BAE9_CHAN_0-7_WR_DMA_PNTR

[0x0018, 48, 78, A8, D8, 108, 138, 168] Write DMA Pointer (write only)

DMA Pointer Address	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 9 PMC-BISERIAL-III BAE9 WRITE DMA POINTER

This write-only port is used to initiate a scatter-gather write DMA. When the physical address of the first chaining descriptor is written to this port, the DMA engine reads four successive long words beginning at that address. The first is the physical address of the first memory block of the DMA buffer containing the data to write to the device, the second is the local address that the data is to be written to, the third is the length in bytes of the block, and the fourth is the physical address of the next chaining descriptor in the list of buffer memory blocks. This process continues until the end-of-chain bit in one of the next pointer values is set, indicating that it is the last descriptor in the list.

Note: Writing a zero to this port will abort a write DMA in progress.

BAE9_CHAN_0-7_TX_ADDRESS

[0x0018, 48, 78, A8, D8, 108, 138, 168] TX RAM Address Offsets (read only)

TX RAM Address Offsets	
Data Bit	**Description**
31-28	Spare
27-16	TX DMA RAM Address Offset
15-12	Spare
11-0	TX I/O RAM Address Offset

FIGURE 10 PMC-BISERIAL-III BAE9 TX RAM ADDRESS OFFSETS

TX I/O RAM Address Offset: This is the long-word address offset of the next word to be read from the transmit RAM and sent by the transmit UART.

TX DMA RAM Address Offset: This is the long-word address offset in the transmit RAM where the next write DMA will start storing data.

BAE9_CHAN_0-7_RD_DMA_PNTR

[0x001C, 4C, 7C, AC, DC, 10C, 13C, 16C] Read DMA Pointer (write only)

DMA Pointer Address	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 11 PMC-BISERIAL-III BAE9 READ DMA POINTER

This write-only port is used to initiate a scatter-gather read DMA. When the physical address of the first chaining descriptor is written to this port, the DMA engine reads four successive long words beginning at that address. The first is the physical address of the first memory block of the DMA buffer where the data from the device will be stored, the second is the local address that the data is read from, the third is the length in bytes of the block, and the fourth is the physical address of the next chaining descriptor in the list of buffer memory blocks. This process continues until the end-of-chain bit in one of the next pointer values is set, indicating that it is the last chaining descriptor in the list.

Note: Writing a zero to this port will abort a read DMA in progress.

BAE9_CHAN_0-7_RX_ADDRESS

[0x001C, 4C, 7C, AC, DC, 10C, 13C, 16C] RX RAM Address Offsets (read only)

RX RAM Address Offsets	
Data Bit	**Description**
31-27	Spare
26-16	RX DMA RAM Address Offset
15-11	Spare
10-0	RX I/O RAM Address Offset

FIGURE 12 PMC-BISERIAL-III BAE9 RX RAM ADDRESS OFFSETS

RX I/O RAM Address Offset: This is the long-word address offset of the next word to be written to the receive RAM after being received by the receive UART.

RX DMA RAM Address Offset: This is the long-word address offset in the receive RAM where the next read DMA will start reading data.

BAE9_CHAN_0-7_IO_ADDR_LAT

[0x0020, 50, 80, B0, E0, 110, 140, 170] TX / RX Latch I/O Start Address (write only)

RX and TX I/O Start Address	
Data Bit	**Description**
31-18	Spare
17	TX Address Latch Strobe
16	RX Address Latch Strobe
15-0	Address to Latch

FIGURE 13 PMC-BISERIAL-III BAE9 RX/TX I/O START ADDRESS

Address to Latch: This 16-bit field specifies the starting long-word address in the transmit or receive RAM where the next I/O operation will start.

RX Address Latch Strobe: When this bit is set to a one, the address value will be loaded into the receive RAM address counter in the receive state-machine. The first location of each message block will contain a status word for that message. Each data-word received will be written to the next RAM location until the message completes. Additional messages will be written to successive memory locations in the same manner. The receive RAM has eleven valid address bits, the upper five bits are ignored.

TX Address Latch Strobe: When this bit is set to a one, the address value will be latched into the transmit address latch of the transmit state-machine. Each message sent loads the latched address into the transmit RAM address counter and the message begins at that address. To send different message data, the latched address must be re-written or the RAM data modified. The transmit RAM has twelve valid address bits, the upper four bits are ignored.

BAE9_CHAN_0-7_TRIG_CNT_LAT

[0x0024, 54, 84, B4, E4, 114, 144, 174] Trigger Monitor Counts Latch (write only)

Trigger Monitor Counts

Data Bit	Description
31-26	Spare
25	Low-Level Minimum Count Latch Strobe
24	Low-Level Maximum Count Latch Strobe
23	High-Level Minimum Count Latch Strobe
22	High-Level Maximum Count Latch Strobe
21-0	Count Value

FIGURE 14 PMC-BISERIAL-III BAE9 TRIGGER MONITOR COUNTS

Count Value: This 22-bit field determines the value of the appropriate limit count that will be latched into the trigger monitor circuit. These counts are used for comparison to actual counts to set latched status bits characterizing the trigger input signal.

High-Level Maximum Count Latch Strobe: When this bit is set to a one, the value of the trigger signal high-level maximum count is latched into the trigger monitor circuit.

High-Level Minimum Count Latch Strobe: When this bit is set to a one, the value of the trigger signal high-level minimum count is latched into the trigger monitor circuit.

Low-Level Maximum Count Latch Strobe: When this bit is set to a one, the value of the trigger signal low-level maximum count is latched into the trigger monitor circuit.

Low-Level Minimum Count Latch Strobe: When this bit is set to a one, the value of the trigger signal low-level maximum count is latched into the trigger monitor circuit.

BAE9_CHAN_0-7_TRIG_HICNT_OUT

[0x0024, 54, 84, B4, E4, 114, 144, 174] Trigger Monitor On Counts (read only)

Trigger Monitor Counts

Data Bit	Description
31-24	Spare
23	Current Signal Level
22	Spare
21-0	High-Level Count Value

FIGURE 15 PMC-BISERIAL-III BAE9 TRIGGER MONITOR ON COUNTS

High-Level Count Value: This 22-bit field reports the number of PLL clock B periods that the last trigger pulse remained at a high level.

Current Signal Level: Reports the level (high or low) of the trigger input signal at the time this register was read.

BAE9_CHAN_0-7_TRIG_LOCNT_OUT

[0x0028, 58, 88, B8, E8, 118, 148, 178] Trigger Monitor Off Counts (read only)

Trigger Monitor Counts

Data Bit	Description
31-24	Spare
23	Current Signal Level
22	Spare
21-0	Low-Level Count Value

FIGURE 16 PMC-BISERIAL-III BAE9 TRIGGER MONITOR OFF COUNTS

Low-Level Count Value: This 22-bit field reports the number of PLL clock B periods that the last trigger pulse remained at a low level.

Current Signal Level: Reports the level (high or low) of the trigger input signal at the time this register was read.

BAE9_CHAN_0-7_DSCRT_OUT_LAT

[0x0028, 58, 88, B8, E8, 118, 148, 178] Discrete Output Parameters (write only)

Discrete Output Signal Parameter

Data Bit	Description
31-25	Spare
24	Duty-Cycle Latch Strobe
23	Period Count Latch Strobe
22	Delay Count Latch Strobe
21-0	Count Value

FIGURE 17 PMC-BISERIAL-III BAE9 DISCRETE OUTPUT PARAMETERS

Count Value: This 22-bit field specifies the number of PLL clock B periods to use for various discrete output signal parameters.

Delay Count Latch Strobe: When this bit is set to a one, the value for the delay count is latched. When operating in a triggered mode, after the trigger is seen, the circuit waits for this count to be reached and then asserts the discrete output signal.

Period Count Latch Strobe: When this bit is set to a one, the value of the period count is latched. In periodic mode, this determines the time between successive assertions of the discrete output signal.

Duty-Cycle Latch Strobe: When this bit is set to a one, the value of the duty-cycle count is latched. This determines the length of the active pulse of the discrete output signal. If this value exceeds the period count, a 50% duty cycle based on the period is used.

BAE9_CHAN_0-7_TX_CONTROL

[0x002C, 5C, 8C, BC, EC, 11C, 14C, 17C] Transmitter Control (read/write)

Transmitter Control

Data Bit	Description
31-16	Spare
15	Level Output Signal Enable
14-13	Discrete Output Mode Select
12	Discrete Output Signal Polarity
11	Discrete Output Trigger Polarity
10	Discrete Output Signal Enable
9-8	Transmit UART Mode Select
7	Transmit Parity Level Select
6	Transmit Odd Parity Select
5	Transmit Parity Enable
4	Transmit Two Stop-Bits Select
3	Transmit Start Clear Enable
2	Transmit UART Trigger Polarity
1	Transmit Done Interrupt Enable
0	Transmitter Enabled (read only)

FIGURE 18 PMC-BISERIAL-III BAE9 TX CONTROL

Transmitter Enabled: When a one is read, the transmit state-machine is enabled; when a zero is read, the state-machine is disabled and the output will be tri-stated.

Transmitter Done Interrupt Enable: When this bit is set to a one, the transmitter done interrupt is enabled. The interrupt will occur when the transmit state-machine completes a message. This will occur when the requested byte count has been reached. At least one byte must be sent to constitute a transmitted message.

Transmit UART Trigger Polarity: When this bit is set to a one, the trigger is set to active-high. When this bit is zero, the trigger is set to active low.

Transmit Start Clear Enable: When this bit is set to a one, the TX start latch will be cleared when the current transmit message completes. When this bit is zero, the TX start latch will remain set until the transmitter is disabled.

Transmit Two Stop-Bits Select: When this bit is set to a one, the transmitter will insert two stop-bits to terminate a data-byte. When this bit is zero, only one stop-bit will be inserted

Transmit Parity Enable: When this bit is set to a one, a parity bit will be added after the eight data-bits and before the stop-bit(s). When this bit is zero, no parity bit will be added.

Transmit Odd Parity Select: When this bit is set to a one, odd parity will be used to determine the value of the parity bit, provided the Parity Level Select bit is a zero. When this bit is zero, even parity will be used.

Transmit Parity Level Select: When this bit is set to a one, the parity bit will be equal to the value of the Odd Parity Select bit. When this bit is zero, the polarity of the parity bit will be calculated using odd or even parity as determined by the Odd Parity Select bit.

Transmit UART Mode Select: This two-bit field specifies the operational mode of the transmit UART as follows:
"00" = Triggered – When enabled the UART waits for the trigger and then the delay;
"01" = Periodic – When enabled the UART message is repeated based on the period;
"10" = One-shot – When enabled the UART immediately sends the message once only;
"11" = Triggered Periodic – The UART operates as in triggered mode, but sends the message repeatedly as in periodic mode.

Discrete Output Signal Enable: When this bit is set to a one, the discrete output signal is enabled. When this bit is zero, the discrete output signal is disabled.

Discrete Output Trigger Polarity: When this bit is set to a one, the discrete output signal trigger is active when it goes high. When this bit is zero, the discrete output signal trigger is active when it goes low.

Discrete Output Signal Polarity: When this bit is set to a one, the discrete output signal is low in the idle state and goes high when active. When this bit is zero, the discrete output signal is high in the idle state and goes low when active.

Discrete Output Mode Select: This two-bit field specifies the operational mode of the discrete output signal as follows:
"00" = Triggered – The signal is idle until the trigger is seen and then the delay expires;
"01" = Periodic – The signal is repeated based on the duty-cycle and period;
"10" = One-shot – The signal immediately outputs one complete cycle, then stays idle;
"11" = Triggered Periodic – The signal is idle until the trigger is seen and the delay is satisfied; then the signal repeats based on the duty-cycle and period.

Level Output Signal Enable: When this bit is set to a one, the discrete output signal will output a steady-state signal. The polarity is controlled by the Discrete Output Signal Polarity bit. The output will be low when the polarity bit is high and high when the polarity bit is low. When this bit is zero, the steady-state output function is disabled.

BAE9_CHAN_0-7_RX_CONTROL

[0x0030, 60, 90, C0, F0, 120, 150, 180] Receiver Control (read/write)

Receiver Control

Data Bit	Description
31-10	Spare
9	Receive Parity Level Select
8	Receive Odd Parity Select
7	Receive Parity Enable
6	Receive Two Stop-Bits Select
5	Receiver Termination Enable
4	Receive Start Clear Enable
3	Framing Error Interrupt Enable
2	Parity Error Interrupt Enable
1	Receive Done Interrupt Enable
0	Receiver Enabled (read only)

FIGURE 19 PMC-BISERIAL-III BAE9 RX CONTROL

Receiver Enabled: When a one is read, the Receive state-machine is enabled and either a message is in progress or it is waiting for a message to begin; when a zero is read, the state-machine is disabled.

Receiver Done Interrupt Enable: When this bit is a one the Receiver interrupt is enabled. The interrupt will occur when the Receive state-machine receives a complete message. This will occur when the at least one byte has been received and then the receive data line is idle for at least eight bit-periods.

Parity Error Interrupt Enable: When this bit is a one the receiver parity error interrupt is enabled. This interrupt will occur when the received parity bit did not match the calculated parity for one or more bytes received. When this bit is zero, the received parity error interrupt is disabled.

Framing Error Interrupt Enable: When this bit is a one the receiver framing error interrupt is enabled. This interrupt will occur when the stop bit(s) polarity or number do not match the expected stop bit(s). When this bit is zero, the framing error interrupt is disabled.

Receive Start Clear Enable: When this bit is set to a one, the RX start latch will be cleared when the current Receive message completes. When this bit is zero, the RX start latch will remain set until the Receiver is disabled.

Receiver Termination Enable: When this bit is set to a one, the 100 Ω receiver I/O shunt termination is enabled when the I/O line is operating in full-duplex mode or in half-duplex mode with the transmitter disabled. This termination is used to reduce noise on the I/O line. If more than one receiver is being driven by the same source, be careful not to enable more than one termination as this could excessively attenuate the signal. When this bit is zero, the termination is disabled.

Receive Two Stop-Bits Select: When this bit is set to a one, the Receiver will expect two stop-bits to terminate a data-byte. When this bit is zero, only one stop-bit will be expected. If the expected stop bits are not received as ones, a framing error will be latched.

Receive Parity Enable: When this bit is set to a one, a parity bit will be expected after the eight data-bits and before the stop-bit(s). When this bit is zero, no parity bit will be expected. If parity is enabled and the parity bit does not match the calculated value, a parity error will be latched.

Receive Odd Parity Select: When this bit is set to a one, odd parity will be used to determine the polarity of the expected parity bit, provided the Parity Level Select bit is a zero. When this bit is zero, even parity will be used.

Receive Parity Level Select: When this bit is set to a one, the expected parity bit will be equal to the value of the Odd Parity Select bit. When this bit is zero, the polarity of the expected parity bit will be calculated using odd or even parity as determined by the Odd Parity Select bit.

BAE9_CHAN_0-7_TX_UART_LATCH

[0x0034, 64, 94, C4, F4, 124, 154, 184] TX UART Parameters (write only)

TX UART Latch

Data Bit	Description
31-19	Spare
18	Bit-Width Latch Strobe
17	TX UART Period Latch Strobe
16	TX UART Delay Latch Strobe
15-0	Delay/Period Count
5-0	Bit-Width

FIGURE 20 PMC-BISERIAL-III BAE9 TX UART PARAMETERS

Bit-Width: This 6-bit field will be latched when the Bit-Width Latch Strobe is asserted. The baud-rate of the UART interface is determined by the latched value and the I/O clock frequency. The valid range of this value is 0x0F – 0x3F, which corresponds to baud rates of 10 Mbps – 2.5 Mbps with a 160 MHz I/O clock. The bit-width field uses the lower six bits of the same field as the delay/period.

Delay/Period Count: This 16-bit field will be latched into the respective latch when either the TX UART Delay Latch Strobe or TX UART Period Latch Strobe is asserted. In triggered modes the delay field specifies the number of I/O bit-periods to wait after the trigger is seen before the transmission starts. In periodic modes the period field specifies the time between the start of subsequent messages. If the message duration exceeds the period, the next message will begin immediately.

TX UART Delay Latch Strobe: When this bit is set to a one, the value for the delay count is latched. When operating in a triggered mode, after the trigger is seen, the transmit state-machine waits for this count to be reached and then sends the transmit UART message.

TX UART Period Latch Strobe: When this bit is set to a one, the value for the period count is latched. In periodic mode, the transmit UART message is repeated at the rate determined by this count. If the message is longer than the count, the message repeats immediately.

Bit-Width Latch Strobe: When this bit is set to a one, the transmit bit-width value is latched. This value can be 0x0F – 0x3F, which results in a bit-width of 16 – 64 I/O clock periods.

BAE9_CHAN_0-7_TX_START_LATCH

[0x0038, 68, 98, C8, F8, 128, 158, 188] TX start (write only)

TX Start Latch

Data Bit	Description
31-17	Spare
16-1	TX Byte Count
0	TX Start

FIGURE 21 PMC-BISERIAL-III BAE9 TX START LATCH

TX Start: When this bit is set to a one, the transmit state-machine will be enabled. When this bit is zero the state-machine will be disabled. The value of the TX start bit is read from the TX_CONTROL register bit 0.

TX Byte Count: This 16-bit field determines the number of bytes to send when the transmitter is enabled.

BAE9_CHAN_0-7_RX_START_LATCH

[0x003C, 6C, 9C, CC, FC, 12C, 15C, 18C] RX start (write only)

RX Start Latch

Data Bit	Description
31-1	Spare
0	RX Start

FIGURE 22 PMC-BISERIAL-III BAE9 RX START LATCH

RX Start: When this bit is set to a one, the receive state-machine will be enabled. When this bit is zero the state-machine will be disabled. The value of the RX start bit is read from the RX_CONTROL register bit 0.

BAE9_CHAN_0-7_RX_BYTE_COUNT

[0x003C, 6C, 9C, CC, FC, 12C, 15C, 18C] RX byte count (read only)

RX Byte Count

Data Bit	Description
31-16	Spare
15-0	RX Bytes Received

FIGURE 23 PMC-BISERIAL-III BAE9 RX BYTE COUNT

RX Bytes Received: This field represents the number of bytes received in the last message. The value will remain valid until the end of a subsequent message. The Receive Done Status/Interrupt can be used to indicate when this value has been updated.

Loop-back

The PMC-BISERIAL-III BAE9 has a 68 pin SCSI II front panel connector. The Engineering kit has reference software, which includes external loop-back tests. Two different test configurations (fixtures) are required to run these tests with the following pins connected.

Full-Duplex Loop-Back

Signal	From	To	Signal
TX0 DATA+	pin 1	pin 2	RX0 DATA+
TX0 DATA-	pin 35	pin 36	RX0 DATA-
TX1 DATA+	pin 3	pin 4	RX1 DATA+
TX1 DATA-	pin 37	pin 38	RX1 DATA-
TX2 DATA+	pin 5	pin 6	RX2 DATA+
TX2 DATA -	pin 39	pin 40	RX2 DATA-
TX3 DATA+	pin 7	pin 8	RX3 DATA+
TX3 DATA-	pin 41	pin 42	RX3 DATA-
TX4 DATA+	pin 9	pin 10	RX4 DATA+
TX4 DATA-	pin 43	pin 44	RX4 DATA-
TX5 DATA+	pin 11	pin 12	RX5 DATA+
TX5 DATA-	pin 45	pin 46	RX5 DATA-
TX6 DATA+	pin 13	pin 14	RX6 DATA+
TX6 DATA -	pin 47	pin 48	RX6 DATA-
TX7 DATA+	pin 15	pin 16	RX7 DATA+
TX7 DATA-	pin 49	pin 50	RX7 DATA-
DISCRETE OUT0+	pin 17	pin 25	DISCRETE INPUT0+
DISCRETE OUT0 -	pin 51	pin 59	DISCRETE INPUT0 -
DISCRETE OUT1+	pin 18	pin 26	DISCRETE INPUT1+
DISCRETE OUT1 -	pin 52	pin 60	DISCRETE INPUT1 -
DISCRETE OUT2+	pin 19	pin 27	DISCRETE INPUT2+
DISCRETE OUT2 -	pin 53	pin 61	DISCRETE INPUT2 -
DISCRETE OUT3+	pin 20	pin 28	DISCRETE INPUT3+
DISCRETE OUT3 -	pin 54	pin 62	DISCRETE INPUT3 -
DISCRETE OUT4+	pin 21	pin 29	DISCRETE INPUT4+
DISCRETE OUT4 -	pin 55	pin 63	DISCRETE INPUT4 -
DISCRETE OUT5+	pin 22	pin 30	DISCRETE INPUT5+
DISCRETE OUT5 -	pin 56	pin 64	DISCRETE INPUT5 -
DISCRETE OUT6+	pin 23	pin 31	DISCRETE INPUT6+
DISCRETE OUT6 -	pin 57	pin 65	DISCRETE INPUT6 -
DISCRETE OUT7+	pin 24	pin 32	DISCRETE INPUT7+
DISCRETE OUT7 -	pin 58	pin 66	DISCRETE INPUT7 -

Half-Duplex Loop-Back

Signal	From	To	Signal
TX/RX 0 DATA+	pin 1	pin 3	TX/RX 1 DATA+
TX/RX 0 DATA-	pin 35	pin 37	TX/RX 1 DATA-
TX/RX 2 DATA+	pin 5	pin 7	TX/RX 3 DATA+
TX/RX 2 DATA -	pin 39	pin 41	TX/RX 3 DATA-
TX/RX 4 DATA+	pin 9	pin 11	TX/RX 5 DATA+
TX/RX 4 DATA-	pin 43	pin 45	TX/RX 5 DATA-
TX/RX 6 DATA+	pin 13	pin 15	TX/RX 7 DATA+
TX/RX 6 DATA -	pin 47	pin 49	TX/RX 7 DATA-
DISCRETE OUT0+	pin 17	pin 27	DISCRETE INPUT2+
DISCRETE OUT0 -	pin 51	pin 61	DISCRETE INPUT2 -
DISCRETE OUT1+	pin 18	pin 28	DISCRETE INPUT3+
DISCRETE OUT1 -	pin 52	pin 62	DISCRETE INPUT3 -
DISCRETE OUT2+	pin 19	pin 29	DISCRETE INPUT4+
DISCRETE OUT2 -	pin 53	pin 63	DISCRETE INPUT4 -
DISCRETE OUT3+	pin 20	pin 30	DISCRETE INPUT5+
DISCRETE OUT3 -	pin 54	pin 64	DISCRETE INPUT5 -
DISCRETE OUT4+	pin 21	pin 31	DISCRETE INPUT6+
DISCRETE OUT4 -	pin 55	pin 65	DISCRETE INPUT6 -
DISCRETE OUT5+	pin 22	pin 32	DISCRETE INPUT7+
DISCRETE OUT5 -	pin 56	pin 66	DISCRETE INPUT7 -
DISCRETE OUT6+	pin 23	pin 33	DISCRETE INPUT8+
DISCRETE OUT6 -	pin 57	pin 67	DISCRETE INPUT8 -
DISCRETE OUT7+	pin 24	pin 34	DISCRETE INPUT9+
DISCRETE OUT7 -	pin 58	pin 68	DISCRETE INPUT9 -

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BISERIAL-III BAE9. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification but not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 24 PMC-BISERIAL-III BAE9 PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BISERIAL-III BAE9. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification but not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 25 PMC-BISERIAL-III BAE9 PN2 INTERFACE

Front Panel I/O Pin Assignment

The figure below gives the pin assignments for the PMC Module I/O Interface on the **PMC-BiSerial-III BAE9.** For a customized version, or other options, contact Dynamic Engineering.

IO_0p	(TX0 DATA +)	IO_0m	(TX0 DATA -)	1	35
IO_1p	(RX0 DATA +)	IO_1m	(RX0 DATA -)	2	36
IO_2p	(TX1 DATA +)	IO_2m	(TX1 DATA -)	3	37
IO_3p	(RX1 DATA +)	IO_3m	(RX1 DATA -)	4	38
IO_4p	(TX2 DATA +)	IO_4m	(TX2 DATA -)	5	39
IO_5p	(RX2 DATA +)	IO_5m	(RX2 DATA -)	6	40
IO_6p	(TX3 DATA +)	IO_6m	(TX3 DATA -)	7	41
IO_7p	(RX3 DATA +)	IO_7m	(RX3 DATA -)	8	42
IO_8p	(TX4 DATA +)	IO_8m	(TX4 DATA -)	9	43
IO_9p	(RX4 DATA +)	IO_9m	(RX4 DATA -)	10	44
IO_10p	(TX5 DATA +)	IO_10m	(TX5 DATA -)	11	45
IO_11p	(RX5 DATA +)	IO_11m	(RX5 DATA -)	12	46
IO_12p	(TX6 DATA +)	IO_12m	(TX6 DATA -)	13	47
IO_13p	(RX6 DATA +)	IO_13m	(RX6 DATA -)	14	48
IO_14p	(TX7 DATA +)	IO_14m	(TX7 DATA -)	15	49
IO_15p	(RX7 DATA +)	IO_15m	(RX7 DATA -)	16	50
IO_16p	(Discrete Out 0 +)	IO_16m	(Discrete Out 0 -)	17	51
IO_17p	(Discrete Out 1 +)	IO_17m	(Discrete Out 1 -)	18	52
IO_18p	(Discrete Out 2 +)	IO_18m	(Discrete Out 2 -)	19	53
IO_19p	(Discrete Out 3 +)	IO_19m	(Discrete Out 3 -)	20	54
IO_20p	(Discrete Out 4 +)	IO_20m	(Discrete Out 4 -)	21	55
IO_21p	(Discrete Out 5 +)	IO_21m	(Discrete Out 5 -)	22	56
IO_22p	(Discrete Out 6 +)	IO_22m	(Discrete Out 6 -)	23	57
IO_23p	(Discrete Out 7 +)	IO_23m	(Discrete Out 7 -)	24	58
IO_24p	(Discrete Input 0 +)	IO_24m	(Discrete Input 0 -)	25	59
IO_25p	(Discrete Input 1 +)	IO_25m	(Discrete Input 1 -)	26	60
IO_26p	(Discrete Input 2 +)	IO_26m	(Discrete Input 2 -)	27	61
IO_27p	(Discrete Input 3 +)	IO_27m	(Discrete Input 3 -)	28	62
IO_28p	(Discrete Input 4 +)	IO_28m	(Discrete Input 4 -)	29	63
IO_29p	(Discrete Input 5 +)	IO_29m	(Discrete Input 5 -)	30	64
IO_30p	(Discrete Input 6 +)	IO_30m	(Discrete Input 6 -)	31	65
IO_31p	(Discrete Input 7 +)	IO_31m	(Discrete Input 7 -)	32	66
IO_32p	(Discrete Input 8 +)	IO_32m	(Discrete Input 8 -)	33	67
IO_33p	(Discrete Input 9 +)	IO_33m	(Discrete Input 9 -)	34	68

FIGURE 26 PMC-BISERIAL-III BAE9 FRONT PANEL INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling the PMC-BISERIAL-III BAE9. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BISERIAL-III BAE9 is constructed out of 0.062-inch thick FR4 material.

Through-hole and surface-mount components are used. The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-BISERIAL-III BAE9 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, then forced-air cooling is recommended. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $125. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois, Suite C
Santa Cruz, CA 95060
(831) 457-8891
Fax (831) 457-4793

support@dyneng.com

Specifications

Host Interface:	[PMC] PCI Mezzanine Card – 32-bit, 33 MHz
Serial Interfaces:	Sixteen UART interfaces (one in and one out per channel). 8-bit data, LSB first, one start-bit, one or two stop-bits and optional parity
TX Bit-rates generated:	Up to 10.4M bits/second; clock reference supplied by the on-board PLL clock A; bit-widths from 16 to 64 I/O clock periods (independently programmable per channel).
Software Interface:	Control Registers, RAMs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory maps)
Wait States:	One for all addresses
Interrupt:	TX message sent, RX message received, RX parity error and RX framing error for each channel
DMA:	16-channel Scatter/Gather DMA support implemented
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module
Construction:	FR4 Multi-Layer Printed Circuit, Through-Hole and Surface-Mount Components
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V
Temperature range	Standard (0 to +70) Extended Temperature available (-40 to +85)

Order Information

PMC-BISERIAL-III BAE9	PMC Module with 8 serial channels, two RS-485 asynchronous I/O per channel (one in and one out); one discrete RS-485 output signal per channel; discrete input used for UART and/or discrete output trigger, each channel selects any one from ten RS-485 inputs
Eng Kit PMC-BISERIAL-III BAE9	HDEterm68 - 68 position screw terminal adapter http://www.dyneng.com/HDEterm68.html HDEcabl68 - 68 I/O twisted pair cable http://www.dyneng.com/HDEcabl68.html Technical Documentation, 1. PMC-BiSerial-III Schematic 2. PMC-BISERIAL-III BAE9 Driver software and user application. Data sheet reprints are available from the manufacturer's web site

Note: *The Engineering Kit is strongly recommended for first time* **PMC-BiSerial-III** *purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. The revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.