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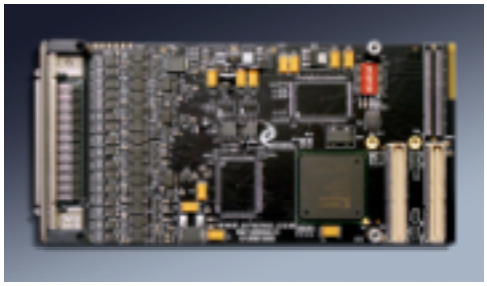
User Manual

PMC-BISERIAL-III LM6

Four-Channel Serial Interface PMC Module



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PMC-BiSerial-III LM6
Four-Channel
PMC Based Serial Interface

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Connection of incompatible hardware is likely to cause serious damage.

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Product Description

The PMC-BiSerial-III LM6 is a part of the PMC Module family of modular I/O products by Dynamic Engineering. It meets the PMC and CMC draft Standards. In standard configuration, the PMC-BiSerial-III LM6 is a Type 1 mechanical with only low profile passive components on the back of the board, one slot wide, with 10 mm inter-board height. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and basic logic design.

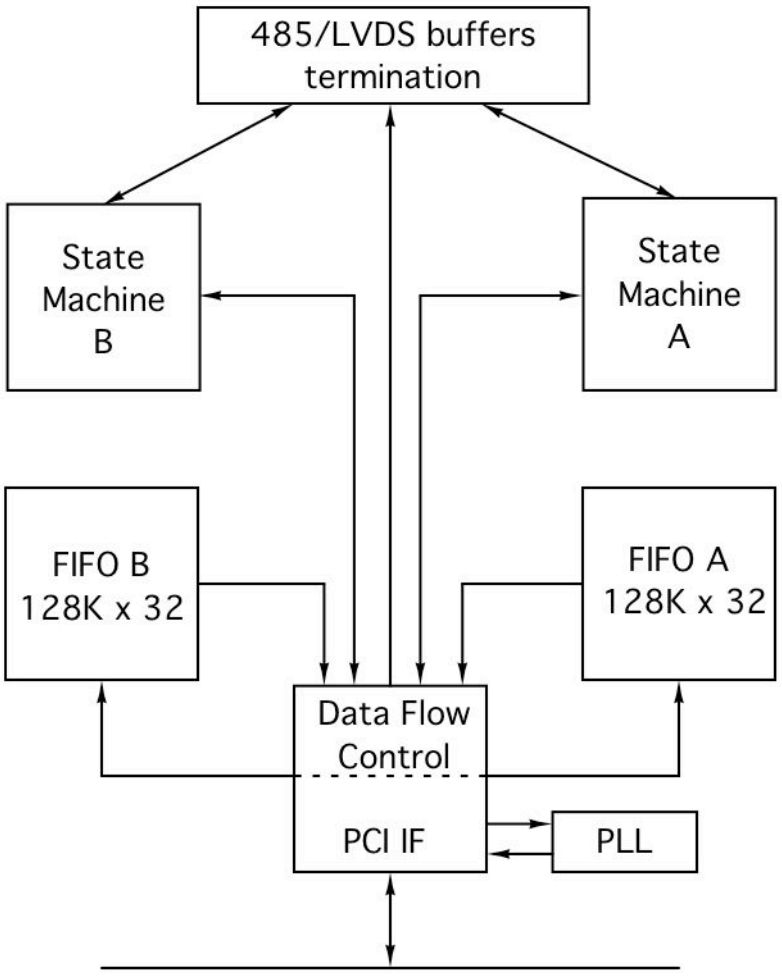


FIGURE 1 PMC-BISERIAL-III BLOCK DIAGRAM

The PMC-BiSerial-III is capable of providing multiple serial protocols using either LVDS or RS-485 I/O standards. The PMC-BiSerial-III standard configuration shown in Figure 1 has two optional data FIFOs that can be as large as 128k x 32-bits to accommodate designs requiring a large amount of buffering. In most designs these FIFOs are not installed and internal FIFOs implemented with the block RAM in the Xilinx FPGA are used instead.

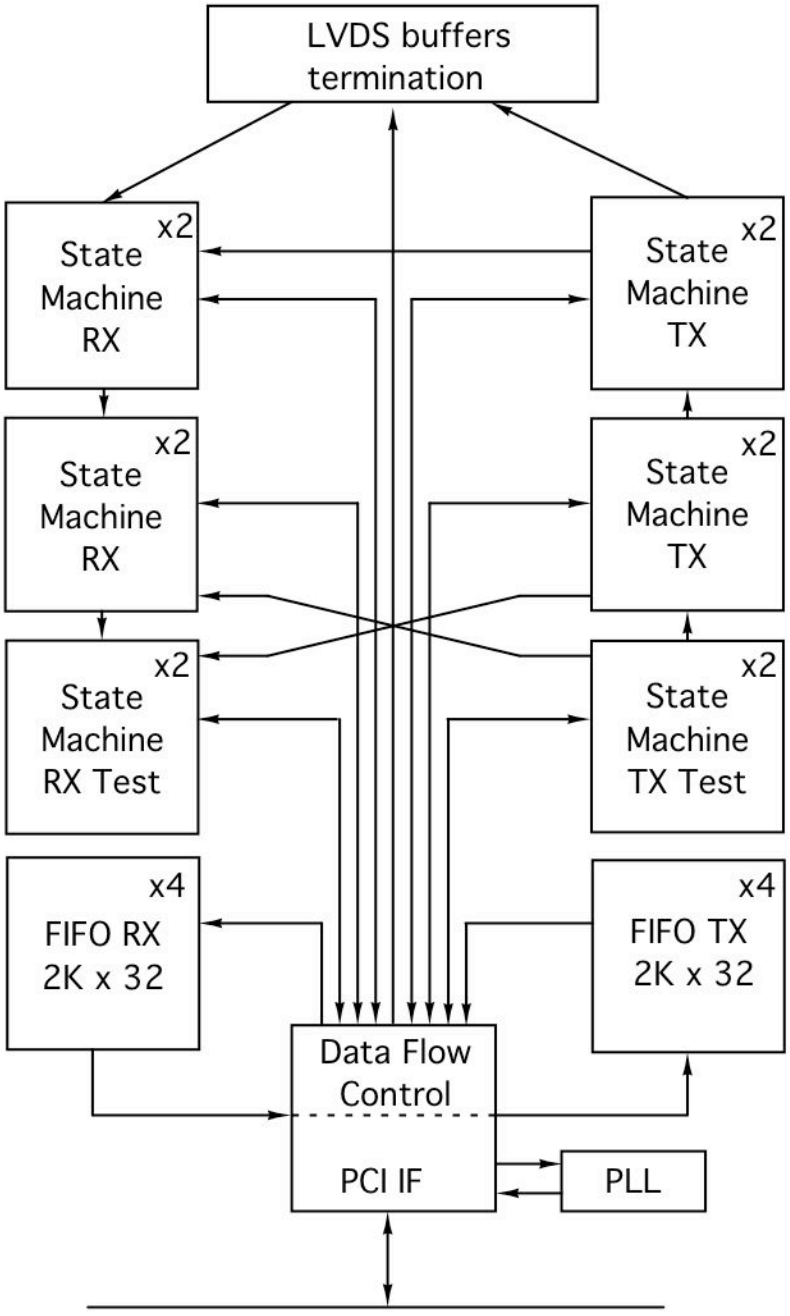


FIGURE 2 PMC-BISERIAL-III LM6 BLOCK DIAGRAM

The PMC-BiSerial-III LM6 configuration is shown in figure 2. The protocol implemented provides four I/O channels each consisting of LVDS transmit and receive data and clock. The on-board PLL is used to generate the two clocks required for the design. The PLL is programmable and uses a 40 MHz reference oscillator to generate a wide range of frequencies. The target rates for this design are 10 Mbits/sec for channels zero and one and 62.5 Mbits/sec for channels two and three.

Data for all channels is received MSB first using start and stop bits to separate data words. Channels zero and one send and receive 36-bit words (packets) consisting of two start bits (‘1’s) a 32-bit data field a parity bit and one stop bit (‘0’) with data changing on the falling edge of the clock (stable on the rising edge). The parity bit is calculated using even parity over the data field. A data frame is terminated with an idle packet consisting of a 36-bit word of all ‘0’s. When no data is being sent, the data line remains in a ‘0’ state.

For stand-alone test purposes, the transmit data from channel one can be internally routed to the channel zero receiver and the channel zero transmit data can be internally routed to the channel one receiver. Since the transmit and receive formats are the same for these channels, no additional I/O logic is required beyond the input multiplexer on the receiver data and clock.

Channels two and three use different formats for transmitted and received data. A transmit packet consists of one start bit (‘1’), a 32-bit data field, an odd parity bit and one stop bit (‘0’) for a total of 35 bits. The received data-word is 66 bits long consisting of one start bit (‘1’), a 64-bit data field and one stop bit (‘1’). Each data-frame begins with a sync word (0x41444364) in the upper-half of the first data word. If this is not seen, data will still be stored, but a framing error will be latched. Parity is not used on this interface. Both interfaces have data changing on the rising edge of the clock (stable on the falling edge).

These channels can also be cross connected as described above for the first two channels. However, since the transmit and receive formats are different, additional transmit and receive test state-machines are needed to interface with the operational I/O state machines.

The LM6 implementation has two 2K by 32-bit FIFOs per channel using the Xilinx internal block RAM, one for the transmitter and one for the receiver. For channels two and three, the same FIFOs are used for data storage regardless of whether the test or operational state-machines are active.

Various interrupts are supported by the PMC-BiSerial-III LM6. An interrupt can be configured to occur when the first receive data is available, at the end of a received or transmitted message, when the transmit FIFO becomes almost empty or when the receive FIFO becomes almost full. Also interrupts can be generated when a parity error occurs or when a framing error occurs or when the receive FIFO overflows (attempt to write to a full FIFO). All interrupts are individually maskable, and a master channel interrupt enable is also provided to disable all interrupts for a channel simultaneously. The current status is available making it possible to operate in a polled mode when interrupts are disabled. All configuration registers support read and write operations for maximum software convenience. All addresses are long word (32-bit) aligned.

Potentially thirty-four differential I/O are available at the front bezel for the serial signals. The drivers and receivers conform to the LVDS specification. The LVDS input signals

are selectively terminated with 100Ω. The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. Optional pullup/pulldown resistor packs can also be installed to provide a logic '1' on undriven lines. This design uses only sixteen of the I/O lines, two in and two out for each of the four channels.

Other custom interfaces are available on request. We will redesign the state machines and create a custom interface protocol that meets your requirements. That protocol will then be offered as a "standard" special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

Since the PMC-BiSerial-III LM6 conforms to the PMC and CMC draft standards, it is guaranteed to be compatibile with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

The PMC-BiSerial-III LM6 uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with the PMC-BiSerial-III LM6, please let us know. We may be able to do a special build with a different height connector to compensate.

Theory of Operation

The PMC-BiSerial-III LM6 features a Xilinx FPGA. The FPGA contains all of the registers, FIFOs and protocol controlling elements of the PMC-BiSerial-III LM6 design. Only the transceivers, switches and PLL circuit are external to the Xilinx device.

A logic block within the Xilinx controls the PCI interface to the host CPU. The PMC-BiSerial-III LM6 design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI core decodes the address and control signals and before the "terminate with data" state is reached. Two additional clock periods account for the delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather DMA is provided for in this design with the memory page information stored in local RAM as a series of chaining descriptors. Once the physical address of the first chaining descriptor is written to the appropriate DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the I/O buffer passed to the read or write call. The next four bytes represent a long-word indicating the length of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to a '1' if this descriptor is the last in the chain. Bit one is set to a '1' if the I/O transfer is from the PMC-BiSerial-III LM6 board to host memory, and a '0' if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one.

To transmit data requires a number of steps to be performed. First, the PLL must be programmed to supply the transmit clocks. Channels zero and one use a 10 MHz clock and channels two and three use a 62.5 MHz clock. The transmitter must be enabled and the data to be sent written to the TX FIFO. The packet count is specified and the send frame latch is set by writing a '1' to the set send frame latch bit in the frame control register. If sufficient data has been written to the FIFO to satisfy the packet count, the transmission will commence. These steps do not need to be performed in this order, but they must all be done to accomplish the transfer.

The exception is the telemetry bus data simulator (channel two or three test transmitter). This interface is intended to send a data-frame several times longer than the amount of data that can be held in the TX FIFO. Therefore the packet count field is ignored and the data-frame will continue until there is no more data to send. In order to accomplish this, the enable and send frame bits should be set first and then an input DMA started that contains all the data to be sent in the data-frame. The transmit state-machine will automatically insert the sync word at the beginning of the frame. The start of transmission will be held off until more than 128 words are in the FIFO to provide a cushion to prevent the FIFO from running dry before the frame has completed.

In order to receive data it is only necessary to enable the receiver and wait for data to be received. The receive state-machine waits for an idle packet to be received before it starts storing a data-frame. This ensures that if a frame is already in progress, the receiver will not store a partial frame. Since the idle state of the data is '0', the requirement for an initial idle packet is easily satisfied as long as the clock is active for a packet time before actual data is sent.

A 16-bit parity error counter is included in each receive channel. This counter will increment each time a parity error is detected in a received data-packet. If the counter ever reaches its maximum count, it will hold that count and not roll-over with a subsequent parity error. The counter is always enabled and will be reset each time the count has been read. The channel two or three normal receive interface does not include a parity bit, so the parity error counter is irrelevant for this interface.

TX FIFO almost empty and RX FIFO almost full levels are programmable by writing values into the respective FIFO level registers**.** Besides generating FIFO level status and potentially causing an interrupt, these values can also be used to give DMA arbitration priority to a FIFO approaching its limit if enabled to do so. This process helps to prevent TX FIFO underrun and RX FIFO overrun when data is being transferred on multiple channels. If a channel FIFO has reached its almost empty/full level, that FIFO will get priority in the DMA arbiter if priority arbitration is enabled for that FIFO.

Programming

Programming the PMC-BiSerial-III LM6 requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BiSerial-III LM6 "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

Before I/O data can be sent or received, the PLL must be programmed to the desired clock configuration. The PLL is connected to the Xilinx by an I^2C serial bus. The PLL internal registers are loaded with 40 bytes of data that are derived from a .jed file generated by the CyberClock utility from Cypress semiconductor. Routines to program the PLL are included in the driver and UserApp code provided in the engineering kit for the board. http://www.dyneng.com/CyberClocks.zip

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the TX/RX interrupts. After an interrupt is received, new TX data can be written or RX data retrieved. An efficient loop can then be implemented to process the data. New messages can be sent or received even as the current one is in progress.

If more than one interrupt is enabled, then the software needs to read the status to see which source caused the interrupt. The status bits are latched, and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status register and write that value back to clear all the latched interrupt status bits before starting a transfer. This will insure that the interrupt status values read by the interrupt service routine came from the current transfer.

If DMA is to be used it will be necessary to acquire blocks of non-paged memory that are accessible from the PCI bus in which to store the DMA chaining descriptor list entries.

Refer to the Theory of Operation section above and the register definition section below for more information regarding the exact sequencing and interrupt definitions.

The PMC-BiSerial-III LM6 VendorId = 0x10EE. The CardId = 0x002D. The device class code is 0x0680 (PCI bridge – other)

Address Map

Register Name	Offset	Description
PB3_LM6_BASE	0x0000	Base Control Register
PB3_LM6_PLL_WRITE	0x0000	Base Control - Bits 16-19 Used for PLL Control
PB3_LM6_PLL_READ	0x0004	Switch Port Bit 19 Used for pll_sdat Input
PB3_LM6_USER_SWITCH	0x0004	User Switch Read Port and Xilinx Design Revision
LM6_CHAN0_CONTROL	0x0010	Channel 0 Control Register
LM6_CHAN0_FRAME	0x0014	Channel 0 Fame Control Register
LM6_CHAN0_STATUS	0x0018	Channel 0 Status Register
LM6_CHAN0_WR_DMA_PNTR	0x001C	Channel 0 Write DMA Physical PCI dpr Address
LM6_CHAN0_TX_FIFO_COUNT	0x001C	Channel 0 TX FIFO Count
LM6_CHAN0_RD_DMA_PNTR	0x0020	Channel 0 Read DMA Physical PCI dpr Address
LM6_CHAN0_RX_FIFO_COUNT	0x0020	Channel 0 RX FIFO Count
LM6_CHAN0_FIFO	0x0024	Channel 0 FIFO Single-Word Access
LM6_CHAN0_TX_AMT_LVL	0x0028	Channel 0 TX almost empty level
LM6_CHAN0_RX_AFL_LVL	0x002C	Channel 0 RX Almost Full Level
LM6_CHAN0_PAR_ERR_COUNT	0x0030	Channel 0 RX Parity Error Count
LM6_CHAN1_CONTROL	0x0038	Channel 1 Control Register
LM6_CHAN1_FRAME	0x003C	Channel 1 Fame Control Register
LM6_CHAN1_STATUS	0x0040	Channel 1 Status Register
LM6_CHAN1_WR_DMA_PNTR	0x0044	Channel 1 Write DMA Physical PCI dpr Address
LM6_CHAN1_TX_FIFO_COUNT	0x0044	Channel 1 TX FIFO Count
LM6_CHAN1_RD_DMA_PNTR	0x0048	Channel 1 Read DMA Physical PCI dpr Address
LM6_CHAN1_RX_FIFO_COUNT	0x0048	Channel 1 RX FIFO Count
LM6_CHAN1_FIFO	0x004C	Channel 1 FIFO Single-Word Access
LM6_CHAN1_TX_AMT_LVL	0x0050	Channel 1 TX Almost Empty Level
LM6_CHAN1_RX_AFL_LVL	0x0054	Channel 1 RX Almost Full Level
LM6_CHAN1_PAR_ERR_COUNT	0x0058	Channel 1 RX Parity Error Count
LM6_CHAN2_CONTROL	0x0060	Channel 2 Control Register
LM6_CHAN2_FRAME	0x0064	Channel 2 Fame Control Register
LM6_CHAN2_STATUS	0x0068	Channel 2 Status Register
LM6_CHAN2_WR_DMA_PNTR	0x006C	Channel 2 Write DMA Physical PCI dpr Address
LM6_CHAN2_TX_FIFO_COUNT	0x006C	Channel 2 TX FIFO Count
LM6_CHAN2_RD_DMA_PNTR	0x0070	Channel 2 Read DMA Physical PCI dpr Address
LM6_CHAN2_RX_FIFO_COUNT	0x0070	Channel 2 RX FIFO Count
LM6_CHAN2_FIFO	0x0074	Channel 2 FIFO Single-Word Access
LM6_CHAN2_TX_AMT_LVL	0x0078	Channel 2 TX Almost Empty Level
LM6_CHAN2_RX_AFL_LVL	0x007C	Channel 2 RX Almost Full Level
LM6_CHAN2_PAR_ERR_COUNT	0x0080	Channel 2 RX Parity Error Count
LM6_CHAN3_CONTROL	0x0088	Channel 3 Control Register
LM6_CHAN3_FRAME	0x008C	Channel 3 Fame Control Register
LM6_CHAN3_STATUS	0x0090	Channel 3 Status Register
LM6_CHAN3_WR_DMA_PNTR	0x0094	Channel 3Write DMA Physical PCI dpr Address
LM6_CHAN3_TX_FIFO_COUNT	0x0094	Channel 3 TX FIFO Count
LM6_CHAN3_RD_DMA_PNTR	0x0098	Channel 3 Read DMA Physical PCI dpr Address
LM6_CHAN3_RX_FIFO_COUNT	0x0098	Channel 3 RX FIFO Count
LM6_CHAN3_FIFO	0x009C	Channel 3 FIFO Single-Word Access
LM6_CHAN3_TX_AMT_LVL	0x00A0	Channel 3 TX Almost Empty Level
LM6_CHAN3_RX_AFL_LVL	0x00A4	Channel 3 RX Almost Full Level
LM6_CHAN3_PAR_ERR_COUNT	0x00A8	Channel 3 RX Parity Error Count

FIGURE 3 PMC-BISERIAL-III LM6 XILINX ADDRESS MAP

Register Definitions

PB3_LM6_BASE

[0x0000] Base Control Register (read/write)

Base Control Register

Data Bit	Description
31-20	Spare
19	PLL Sdata Output
18	PLL S2 Output
17	PLL Sclk Output
16	PLL Enable
15-0	Spare

FIGURE 4 PMC-BISERIAL-III LM6 BASE CONTROL REGISTER

All bits are active high and are reset on power-up or reset command, except PLL enable, which defaults to enabled (high) on power-up or reset.

PLL Enable: When this bit is set to a one, the signals used to program and read the PLL are enabled.

PLL Sclk/Sdata Output: These signals are used to program the PLL over the I^2C serial interface. Sclk is always an output whereas Sdata is bi-directional. This register is where the Sdata output value is specified. When Sdata is an input it is read from the User Switch Port.

PLL S2 Output: This is an additional control line to the PLL that can be used to select additional pre-programmed frequencies.

PB3_LM6_USER_SWITCH

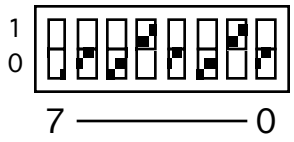
[0x0004] User Switch Port (read only)

Dip-Switch Port

Data Bit	Description
31-20	Spare
19	PLL Sdata Input
18-16	Spare
15-8	Xilinx Design Revision Number
7-0	Switch Setting

FIGURE 5 PMC-BISERIAL-III LM6 USER SWITCH PORT

Switch Setting: The user switch is read through this port. The bits are read as the lowest byte in the port. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



Xilinx Design Revision Number: The value of the second byte of this port is the rev. number of the Xilinx design (currently 0x04 - rev. D).

PLL Sdata Input: The PLL_sdata bi-directional line is read using this bit. This line is used to read the register contents of the PLL.

LM6_CHAN0-3_CONTROL

[0x0010, 0x0038, 0x0060, 0x0088] Channel Control Register (read/write)

Channel Control Register

Data Bit	Description
31-24	Spare
23	Receive Test Mode Select
22	Transmit Test Mode Select
21	Receive Test Input Select
20	Receive Termination Enable
19	Read DMA Interrupt Enable
18	Write DMA Interrupt Enable
17	Receive DMA Priority Arbitration Enable
16	Transmit DMA Priority Arbitration Enable
15	RX FIFO Almost Full Interrupt Enable
14	Receive FIFO Overflow Interrupt Enable
13	Receive Framing Error Interrupt Enable
12	Receive Parity Error Interrupt Enable
11	Receive Done Interrupt Enable
10	Receive Data Available Interrupt Enable
9	TX FIFO Almost Empty Interrupt Enable
8	Transmit Done Interrupt Enable
7	Transmit Send Frame Clear Enable
6	Receive Enable
5	Transmit Enable
4	Force Interrupt
3	Master Interrupt Enable
2	FIFO Bypass Enable
1	Receive FIFO Reset
0	Transmit FIFO Reset

FIGURE 6 PMC-BISERIAL-III LM6 CHANNEL CONTROL REGISTER

Transmit/Receive FIFO Reset: When these bits are set to a one, the transmit and/or receive FIFOs will be reset. When these bits are zero, normal FIFO operation is enabled.

FIFO Bypass Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without using the I/O. When this bit is zero, normal FIFO operation is enabled.

Master Interrupt Enable: When this bit is set to a one, all enabled interrupts (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one, a system interrupt will occur provided the master interrupt enable is set. This is useful for interrupt testing.

Transmit Enable: When this bit is set to a one, the transmit state-machine will be enabled. I/O data will not be sent unless sufficient data has been written to the TX FIFO to satisfy the transmit packet count and the send frame latch has been set. When this bit is a zero the transmitter is disabled.

Receive Enable: When this bit is set to a one, the receiver is enabled and will start to look for received serial data. When this bit is zero, the receiver is disabled.

Transmit Send Frame Clear Enable: When this bit is set to a one, the send frame latch will be cleared when the current transmit frame completes. When this bit is zero, the send frame latch will remain set until explicitly cleared or the transmitter is disabled.

Transmit Done Interrupt Enable: When this bit is set to a one, the transmit interrupt is enabled. A transmit interrupt will be asserted when a data-frame has been completely sent, provided the master interrupt enable is asserted. When this bit is zero, the transmit interrupt is disabled.

TX FIFO Almost Empty Interrupt Enable: When this bit is set to a one, the transmit FIFO almost empty interrupt is enabled. An interrupt will be asserted when the FIFO level becomes less than or equal to the count in the LM6_CHAN0-3_TX_AMT_LVL register, provided the master interrupt enable is asserted. When this bit is zero, the transmit FIFO almost empty interrupt is disabled.

Receive Data Available Interrupt Enable: When this bit is set to a one, the receive data available interrupt is enabled. An interrupt will be asserted, provided the master interrupt is enabled when the first data-word has been received. When this bit is zero, the receive data available interrupt is disabled.

Receive Done Interrupt Enable: When this bit is set to a one, the receiver done interrupt is enabled. An interrupt will be asserted, provided the master interrupt is enabled when at least one complete data-frame has been received. When this bit is zero, the receiver done interrupt is disabled.

Receive Parity Error Interrupt Enable: When this bit is set to a one, the receive parity error interrupt is enabled. An interrupt will be asserted, provided the master interrupt is enabled when the receiver detects a parity error in one of the data packets. When this bit is zero, the receive parity error interrupt is disabled.

Receive Framing Error Interrupt Enable: When this bit is set to a one, the receive framing error interrupt is enabled. An interrupt will be asserted, provided the master interrupt is enabled when the receiver detects a framing error in one of the data packets. This will occur if the stop bit received is not a ‘0’ or in the case of the telemetry

bus, if the correct sync word is not seen at the beginning of the frame. When this bit is zero, the receive framing error interrupt is disabled.
Receive FIFO Overflow Interrupt Enable: When this bit is set to a one, the receive FIFO overflow interrupt is enabled. An interrupt will be asserted, provided the master interrupt is enabled when an attempt is made to write to a full receive FIFO. When this bit is zero, the receive FIFO overflow interrupt is disabled.

RX FIFO Almost Full Interrupt Enable: When this bit is set to a one, the receive FIFO almost full interrupt is enabled. An interrupt will be asserted when the FIFO level becomes greater than or equal to the count in the LM6_CHAN0-3_RX_AFL_LVL register, provided the master interrupt enable is asserted. When this bit is zero, the RX FIFO almost full interrupt is disabled.

Transmit / Receive DMA Priority Arbitration Enable: When this bit is set to a one, the corresponding DMA channel will get priority if it is near the limit of its FIFO (almost empty for the TX or almost full for the RX). These limits are derived from the programmable counts in the LM6_CHAN0-3_TX_AMT_LVL and LM6_CHAN0-3_RX_AFL_LVL registers.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA writes and reads respectively. The DMA interrupts are not affected by the Master Interrupt Enable.

Receive Termination Enable: When this bit is set to a one, the 100 Ω receiver I/O shunt termination is enabled. This termination is used to reduce noise on the I/O line. If more than one receiver is being driven by the same source, be careful not to enable more than one termination as this could excessively attenuate the signal. When this bit is zero, the termination is disabled.

Receive Test Input Select: This bit is valid for all channels. When it is set to a one, the data and clock inputs to the receiver are routed internally from the appropriate transmitter (TX 1 for channel 0, TX 0 for channel 1, TX 3 for channel 2 or TX 2 for channel 3). When this bit is zero, the data and clock inputs come from the external LVDS receivers.

Transmit Test Mode Select: This bit is only used by channel two or three. When it is set to a one, the test transmit state-machine (66-bit packet) is active. When this bit is zero, the operational transmit state-machine is active.

Receive Test Mode Select: This bit is only used by channel two or three. When it is set to a one, the test receive state-machine (35-bit packet) is active. When this bit is zero, the operational receive state-machine is active.

LM6_CHAN0-3_FRAME

[0x0014, 0x003C, 0x0064, 0x008C] Frame Control Register (write only)

Frame Control Register

Data Bit	Description
31-18	Spare
17	Clear Send-Frame Latch
16	Set Send-Frame Latch
15-11	Spare
10-0	Transmit Packet Count

FIGURE 7 PMC-BISERIAL-III LM6 CHANNEL CONTROL REGISTER

Transmit Packet Count: This field specifies the number of transmit data-packets to be sent in a data-frame. The transmit state-machine will wait until there are at least this many words in the transmit FIFO before starting a frame transmission. The field width is 11 bits for a maximum frame size of 2047 packets. This field is not used by the telemetry bus simulator (channel 2 or 3 test transmitter), which sends frames much longer than can be contained in the FIFO. In this case data is sent until there is insufficient data left in the FIFO to construct a data packet (less than two 32-bit words). This state-machine will not begin transmission until there are more than 128 words in the FIFO in order to establish a cushion to avoid running out of data prematurely. The frame data must be written to the FIFO as the frame transmission is in progress.

Set Send-Frame Latch: This bit sets the send-frame latch that is read from the channel status port.

Clear Send-Frame Latch: This bit clears the send-frame latch that is read from the channel status port. The latch can also be cleared automatically when a transmit data-frame completes if the transmit send-frame clear bit is set. It will also be cleared if the transmitter is disabled.

LM6_CHAN0-3_STATUS

[0x0018, 0x0040, 0x0068, 0x0090] Channel Status Read/Clear Latch Write Port

Channel Status Register

Data Bit	Description
31	Channel Interrupt Active
30-25	Spare
24	User Interrupt Condition Occurred
23-22	Spare
21	Transmit Send-Frame Active
20	Receive Clock Lost
19	Read DMA Interrupt Occurred
18	Write DMA Interrupt Occurred
17	Read DMA Error Occurred
16	Write DMA Error Occurred
15	RX FIFO Almost Full Interrupt Occurred
14	Receive FIFO Overflow Occurred
13	Receive Framing Error Occurred
12	Receive Parity Error Occurred
11	Receiver Done Interrupt Occurred
10	Receive Data Available Interrupt Occurred
9	TX FIFO Almost Empty Interrupt Occurred
8	Transmit Interrupt Occurred
7	Receive Data Valid
6	Receive FIFO Full
5	Receive FIFO Almost Full
4	Receive FIFO Empty
3	Spare
2	Transmit FIFO Full
1	Transmit FIFO Almost Empty
0	Transmit FIFO Empty

FIGURE 8 PMC-BISERIAL-III LM6 CHANNEL STATUS PORT

Transmit FIFO Empty: When a one is read, the transmit data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Transmit FIFO Almost Empty: When a one is read, the number of data words in the transmit data FIFO is less than or equal to the value written to the LM6_CHAN_TX_AMT_LVL register; when a zero is read, the FIFO level is more than that value.

Transmit FIFO Full: When a one is read, the transmit data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive FIFO Empty: When a one is read, the receive data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data words in the receive data FIFO is greater or equal to the value written to the LM6_CHAN_RX_AFL_LVL register; when a zero is read, the FIFO level is less than that value.

Receive FIFO Full: When a one is read, the receive data FIFO is full; when a zero is read, there is room for at least one more data-word in the FIFO.

Receive Data Valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO is empty, because as soon as the first four words are written into the FIFO, they are read out to fill the receive data pipe-line to be ready for a PCI read DMA or single word access. When this bit is a zero, it indicates that there is no valid receive data remaining.

Transmit Interrupt Occurred: When a one is read, it indicates that the transmit state-machine sent at least one data-frame. A zero indicates that a data-frame has not been sent. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

TX FIFO Almost Empty Interrupt Occurred: When a one is read, it indicates that the TX FIFO has become less than or equal to the value in the LM6_CHAN_TX_AMT_LVL register. A zero indicates that the FIFO has not become almost empty. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Data Available Interrupt Occurred: When a one is read, it indicates that the receive state-machine has received the first packet of a data-frame. A zero indicates that no data has been received. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receiver Done Interrupt Occurred: When a one is read, it indicates that the receive state-machine has received at least one complete data-frame. A zero indicates that a data-frame has not been received. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Parity Error Occurred: When a one is read, it indicates that a parity error was detected in a received data-packet. A zero indicates that no parity error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Receive Framing Error Occurred: When a one is read, it indicates that a framing error has been detected in the receive data stream. This is caused by an incorrect stop bit or if the correct sync word was not received on the telemetry bus. A zero indicates that no framing error has occurred. This bit is latched and can be cleared by writing back to the

Status register with a one in this bit position.
Receive FIFO Overflow Occurred: When a one is read, it indicates that an attempt has been made to write data to a full receive data FIFO. A zero indicates that no overflow condition has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

RX FIFO Almost Full Interrupt Occurred: When a one is read, it indicates that the RX FIFO has become greater than or equal to the value in the LM6_CHAN_RX_AFL_LVL register. A zero indicates that the FIFO has not become almost full. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Write/Read DMA Error Occurred: When a one is read, a write or read DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is incorrect. A zero indicates that no write or read DMA error has occurred. These bits are latched and can be cleared by writing back to the Status register with a one in the appropriate bit position.

Write/Read DMA Interrupt Occurred: When a one is read, a write/read DMA interrupt is latched. This indicates that the scatter-gather list for the current write or read DMA has completed, but the associated interrupt has yet to be processed. A zero indicates that no write or read DMA interrupt is pending.

Receive Clock Lost: When a one is read, it indicates that the receive clock has become inactive. This bit is only valid for channel two or three. A zero indicates that the receive clock has remained active. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Transmit Send-Frame Active: When a one is read, it indicates that the active transmit state-machine is currently sending or waiting to send a data-frame. A zero indicates that no transmit data-frame is active or pending.

User Interrupt Condition Occurred: When a one is read, it indicates that an enabled user interrupt condition has occurred. These conditions include the TX and RX state-machine and FIFO interrupts as well as the RX parity error, framing error and FIFO overflow interrupts. Also the Force Interrupt bit will cause this bit to be asserted. A system interrupt will occur if the Master Interrupt Enable is set. A zero indicates that no enabled user interrupt condition is active.

Channel Interrupt Active: When a one is read, it indicates that a system interrupt is asserted caused by an enabled channel interrupt condition. A zero indicates that no system interrupt is pending from an enabled channel interrupt condition

LM6_CHAN0-3_WR_DMA_PNTR

[0x001C, 0x0044, 0x006C, 0x0094] Write DMA Pointer (write only)

DMA Pointer Address Register	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 9 PMC-BISERIAL-III LM6 WRITE DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather write DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer containing the data to write to the device, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

Note: Writing a zero to this port will abort a write DMA in progress.

LM6_CHAN0-3_TX_FIFO_COUNT

[0x001C, 0x0044, 0x006C, 0x0094] TX FIFO data count (read only)

TX FIFO Data Count Port	
Data Bit	**Description**
31-12	Spare
11-0	TX Data Words Stored

FIGURE 10 PMC-BISERIAL-III LM6 TX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the transmit FIFO and data holding register (currently a maximum of 0x801).

LM6_CHAN0-3_RD_DMA_PNTR

[0x0020, 0x0048, 0x0070, 0x0098] Read DMA Pointer (write only)

DMA Pointer Address Register	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 11 PMC-BISERIAL-III LM6 READ DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather read DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer where the data from the device will be stored, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

Note: Writing a zero to this port will abort a read DMA in progress.

LM6_CHAN0-3_RX_FIFO_COUNT

[0x0020, 0x0048, 0x0070, 0x0098] RX FIFO data count (read only)

RX FIFO Data Count Port	
Data Bit	**Description**
31-12	Spare
11-0	RX Data Words Stored

FIGURE 12 PMC-BISERIAL-III LM6 RX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the receive FIFO and data pipeline (currently a maximum of 0x804).

LM6_CHAN0-3_FIFO

[0x0024, 0x004C, 0x0074, 0x009C] Write TX/Read RX FIFO Port

RX and TX FIFO Port	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 13 PMC-BISERIAL-III LM6 RX/TX FIFO PORT

This port is used to make single-word accesses into the TX and out of the RX FIFO.

LM6_CHAN0-3_TX_AMT_LVL

[0x0028, 0x0050, 0x0078, 0x00A0] TX almost-empty level (read/write)

TX Almost-Empty Level Register	
Data Bit	**Description**
31-16	Spare
15-0	TX FIFO Almost-Empty Level

FIGURE 14 PMC-BISERIAL-III LM6 TX ALMOST EMPTY LEVEL REGISTER

This read/write port accesses the transmitter almost-empty level register. When the number of data words in the transmit data FIFO is equal or less than this value, the almost-empty status bit is set.

LM6_CHAN0-3_RX_AFL_LVL

[0x002C, 0x0054, 0x007C, 0x00A4] RX almost-full level (read/write)

RX Almost-Full Level Register	
Data Bit	**Description**
31-16	Spare
15-0	RX FIFO Almost-Full Level

FIGURE 15 PMC-BISERIAL-III LM6 RX ALMOST FULL LEVEL REGISTER

This read/write port accesses the receiver almost-full level register. When the number of data words in the receive data FIFO is equal or greater than this value, the almost-full status bit is set.

LM6_CHAN0-3_PAR_ERR_COUNT

[0x0030, 0x0058, 0x0080, 0x00A8] RX Parity error count (read only)

Parity Error Count Port

Data Bit	Description
31-16	Spare
15-0	Parity Errors Detected

FIGURE 16 PMC-BISERIAL-III LM6 PARITY ERROR COUNT PORT

This read-only register port reports the number of parity errors detected in received data packets. If the count reaches the maximum, this value will be held. The counter will not roll-over. The count will be cleared when this port is read.

Loop-back

The Engineering kit has reference software, which includes external loop-back tests. The PMC-BISERIAL-III LM6 has a 68 pin SCSI II front panel connector. The tests require an external cable with the following pins connected.

Signal	From	To	Signal
TX0 DATA+	pin 1	pin 25	RX0 DATA+
TX0 DATA-	pin 35	pin 59	RX0 DATA-
TX0 CLOCK+	pin 2	pin 26	RX0 CLOCK+
TX0 CLOCK-	pin 36	pin 60	RX0 CLOCK-
TX1 DATA+	pin 3	pin 27	RX1 DATA+
TX1 DATA-	pin 37	pin 61	RX1 DATA-
TX1 CLOCK+	pin 4	pin 28	RX1 CLOCK+
TX1 CLOCK-	pin 38	pin 62	RX1 CLOCK-
TX2 DATA+	pin 5	pin 29	RX2 DATA+
TX2 DATA -	pin 39	pin 63	RX2 DATA-
TX2 CLOCK+	pin 6	pin 30	RX2 CLOCK+
TX2 CLOCK -	pin 40	pin 64	RX2 CLOCK-
TX3 DATA+	pin 7	pin 31	RX3 DATA+
TX3 DATA-	pin 41	pin 65	RX3 DATA-
TX3 CLOCK+	pin 8	pin 32	RX3 CLOCK+
TX3 CLOCK-	pin 42	pin 66	RX3 CLOCK-

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BISERIAL-III LM6. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification but not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 17 PMC-BISERIAL-III LM6 PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BISERIAL-III LM6. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification but not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 18 PMC-BISERIAL-III LM6 PN2 INTERFACE

Front Panel I/O Pin Assignment

The figure below gives the pin assignments for the PMC Module I/O Interface on the **PMC-BiSerial-III LM6.** For a customized version, or other options, contact Dynamic Engineering.

IO_0p (TX0 DATA+)	IO_0m (TX0 DATA-)	1	35
IO_1p (TX0 CLK+)	IO_1m (TX0 CLK-)	2	36
IO_2p (TX1 DATA+)	IO_2m (TX1 DATA-)	3	37
IO_3p (TX1 CLK+)	IO_3m (TX1 CLK-)	4	38
IO_4p (TX2 DATA+)	IO_4m (TX2 DATA-)	5	39
IO_5p (TX2 CLK+)	IO_5m (TX2 CLK-)	6	40
IO_6p (TX3 DATA+)	IO_6m (TX3 DATA-)	7	41
IO_7p (TX3 CLK+)	IO_7m (TX3 CLK-)	8	42
IO_8p	IO_8m	9	43
IO_9p	IO_9m	10	44
IO_10p	IO_10m	11	45
IO_11p	IO_11m	12	46
IO_12p	IO_12m	13	47
IO_13p	IO_13m	14	48
IO_14p	IO_14m	15	49
IO_15p	IO_15m	16	50
IO_16p	IO_16m	17	51
IO_17p	IO_17m	18	52
IO_18p	IO_18m	19	53
IO_19p	IO_19m	20	54
IO_20p	IO_20m	21	55
IO_21p	IO_21m	22	56
IO_22p	IO_22m	23	57
IO_23p	IO_23m	24	58
IO_24p (RX0 DATA+)	IO_24m (RX0 DATA-)	25	59
IO_25p (RX0 CLK+)	IO_25m (RX0 CLK-)	26	60
IO_26p (RX1 DATA+)	IO_26m (RX1 DATA-)	27	61
IO_27p (RX1 CLK+)	IO_27m (RX1 CLK-)	28	62
IO_28p (RX2 DATA+)	IO_28m (RX2 DATA-)	29	63
IO_29p (RX2 CLK+)	IO_29m (RX2 CLK-)	30	64
IO_30p (RX3 DATA+)	IO_30m (RX3 DATA-)	31	65
IO_31p (RX3 CLK+)	IO_31m (RX3 CLK-)	32	66
IO_32p	IO_32m	33	67
IO_33p	IO_33m	34	68

FIGURE 19 PMC-BISERIAL-III LM6 FRONT PANEL INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling the PMC-BISERIAL-III LM6. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BISERIAL-III LM6 is constructed out of 0.062-inch thick FR4 material.

Through-hole and surface-mount components are used. The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-BISERIAL-III LM6 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, then forced-air cooling is recommended. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois, Suite C
Santa Cruz, CA 95060
(831) 457-8891 Fax (831) 457-4793
support@dyneng.com

Specifications

Host Interface:	[PMC] PCI Mezzanine Card – 32-bit, 33 MHz
Serial Interfaces:	Sixteen serial interfaces (two in and two out per channel). 35, 36 and 66-bit word sizes, MSB first
TX Bit-rates generated:	10 Mbits/second for TX and RX serial channels 0 and 1 62.5 Mbits/second for TX and RX serial channels 2 and 3 clock references supplied by the on-board PLL
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory map)
Wait States:	One for all addresses
Interrupt:	TX data-block sent, RX data-block received, RX parity error, RX framing error and RX FIFO overflow
DMA:	Multi-channel Scatter/Gather DMA support implemented
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module
Construction:	FR4 Multi-Layer Printed Circuit, Through-Hole and Surface-Mount Components
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V
Temperature range	Standard (0 to +70) Extended Temperature available (-40 to +85)

Order Information

PMC-BISERIAL-III LM6	PMC Module with 4 serial channels, four LVDS I/O per channel (two in and two out)
Eng Kit PMC-BISERIAL-III LM6	HDEterm68 - 68 position screw terminal adapter http://www.dyneng.com/HDEterm68.html HDEcabl68 - 68 I/O twisted pair cable http://www.dyneng.com/HDEcabl68.html Technical Documentation, 1. PMC-BiSerial-III Schematic 2. PMC-BISERIAL-III LM6 Driver software and user application. Data sheet reprints are available from the manufacturer's web site

***Note**: The Engineering Kit is strongly recommended for first time* **PMC-BiSerial-III** *purchases.*

PMC's can be adapted into many system architectures including PCI, PCIe, cPCI, PC104p and VME. Dynamic Engineering has solutions for your carrier requirements. Please visit the Dynamic Engineering Website for a complete list of adapters for PMC and other mezzanine products. http://www.dyneng.com

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. The revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.