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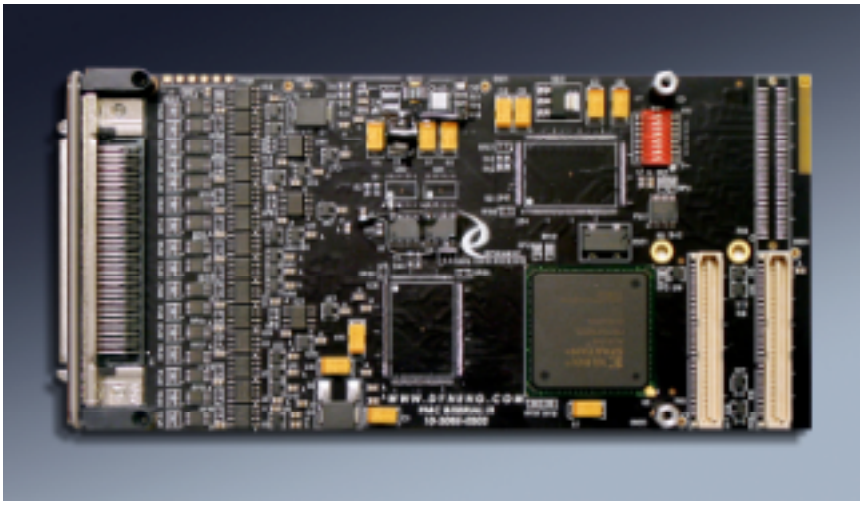
User Manual

PMC-BISERIAL-III MDS1

Four-Channel Manchester Encoded Serial Interface PMC Module



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PMC-BiSerial-III MDS1
Four-Channel Manchester-Encoded
PMC Based Serial Interface

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Product Description

The PMC-BiSerial-III MDS1 is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC-BiSerial-III is capable of providing multiple serial protocols using either LVDS or RS-485 I/O standards.

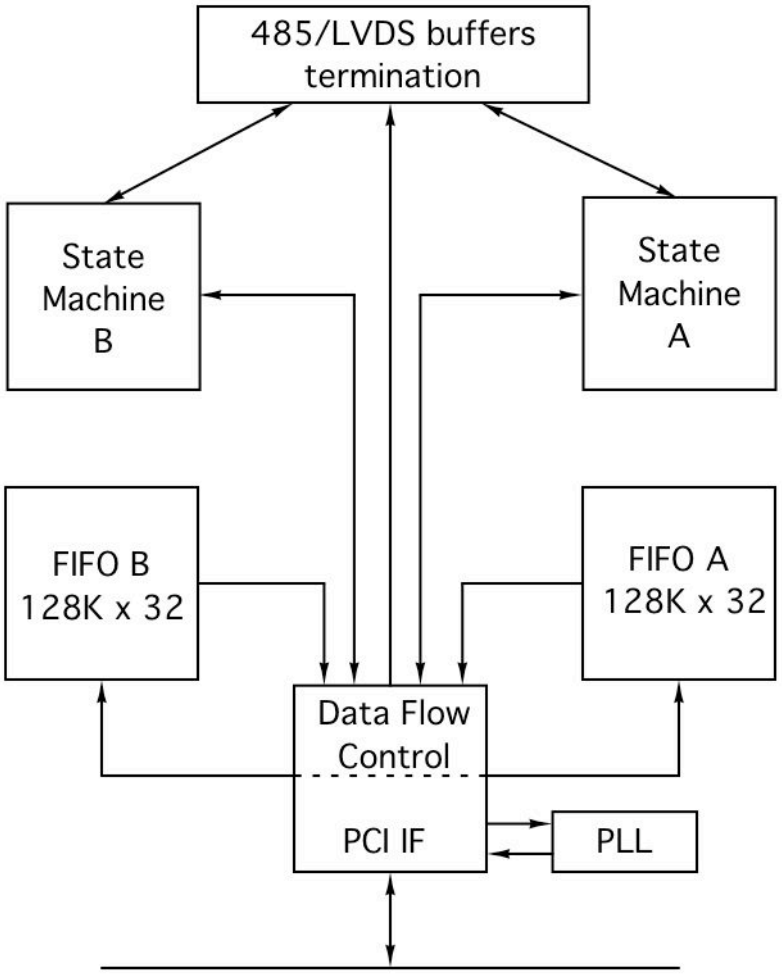


FIGURE 1 PMC-BISERIAL-III BLOCK DIAGRAM

The PMC-BiSerial-III standard configuration shown in Figure 1 has two optional data FIFOs that can be as large as 128k x 32-bit to accommodate designs requiring a large amount of buffering. In most designs these FIFOs are not installed and internal FIFOs implemented using the block RAM in the Xilinx FPGA are used instead.

The MDS1 protocol implemented provides four channels each consisting of an RS-485 transmit data and receive data using Manchester encoding. The on-board PLL is used to generate the two clocks required for the design. The PLL is programmable and uses

a 40 MHz reference oscillator to generate a wide range of frequencies. The target rate for this design is 192 kbits/sec. The transmitter uses a double-rate clock to encode the Manchester output and the receiver uses an eight times clock to detect and decode the Manchester input. The receiver can adapt to a range of frequencies from approximately 0.75 to 1.25 of the target frequency.

Other custom interfaces are available on request. We will redesign the state machines and create a custom interface protocol that meets your requirements. That protocol will then be offered as a "standard" special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

The MDS1 implementation has two 1K by 32-bit FIFOs using the Xilinx internal block RAM, one for the transmitter and one for the receiver. Data is received MSB first in blocks of 81 16-bit words. Each data-block is preceded by a 16-bit sync pattern (0xAAAA). The idle time between data blocks is approximately 20 milliseconds and is filled with Manchester encoded zero's.

All 81 data words end with a binary 01 tag sequence which leaves 14 significant bits of data. The first 80 words in the data-block are thermocouple voltages represented in floating point format. The 81st word contains the 8-bit unit ID in bits 14-7.

The transmitter is used only for testing the receiver which is the focus of the design. The transmitter will send data when it is enabled and there are at least 41 32-bit words in the transmit FIFO. It sends the 16-bit sync pattern and then sends 81 16-bit words starting with the lower half of the first 32-bit FIFO word followed by the upper half. Only the lower half of the 41st FIFO word is sent; the upper half is discarded.

Thirty-four differential I/O are available at the front bezel for the serial signals. The drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are selectively terminated with 100Ω. The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. Optional pullup/pulldown resistor packs can also be installed to provide a logic '1' on undriven lines.
This design uses only eight of the I/O lines, one in and one out for each of the four channels.

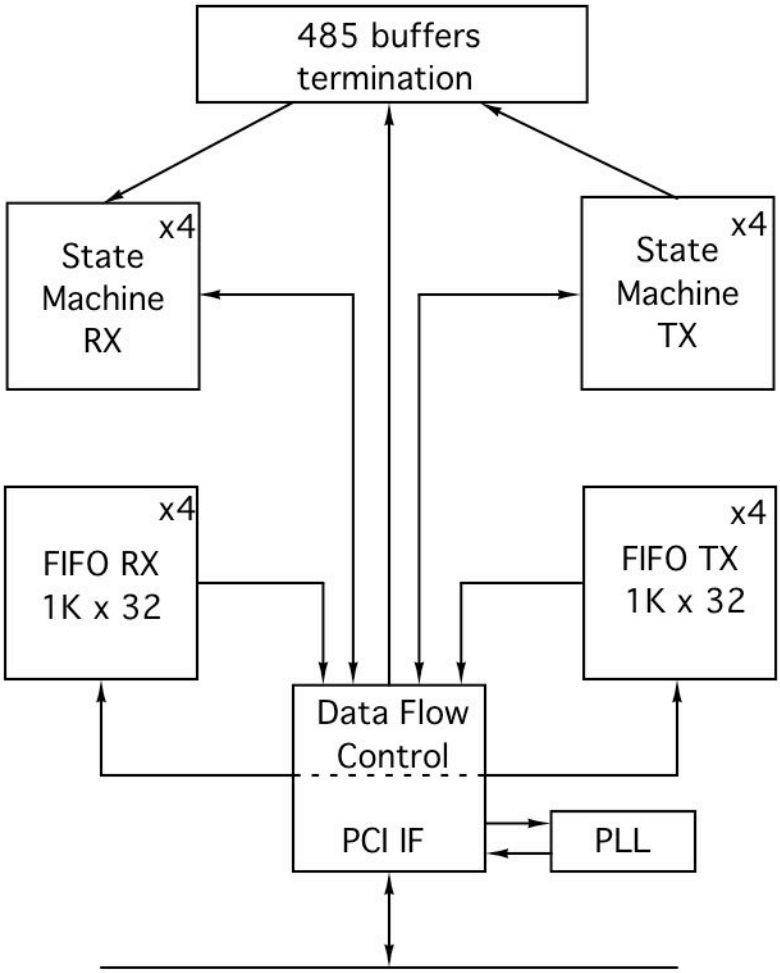


FIGURE 2 PMC-BISERIAL-III MDS1 BLOCK DIAGRAM

The PMC-BiSerial-III MDS1 conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

The PMC-BiSerial-III MDS1 uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with the PMC-BISERIAL-III MDS1, please let us know. We may be able to do a special build with a different height connector to compensate.

Various interrupts are supported by the PMC-BiSerial-III MDS1. An interrupt can be

configured to occur at the end of a received or transmitted message. Also interrupts can be generated when the receiver is inactive for more than four bit periods or when the receive FIFO overflows (attempt to write to a full FIFO). All interrupts are individually maskable, and a master channel interrupt enable is also provided to disable all interrupts for a channel simultaneously. The current status is available making it possible to operate in a polled mode when interrupts are disabled. All configuration registers support read and write operations for maximum software convenience. All addresses are long word (32-bit) aligned.

Theory of Operation

The PMC-BISERIAL-III MDS1 features a Xilinx FPGA. The FPGA contains all of the registers, FIFOs and protocol controlling elements of the PMC-BISERIAL-III MDS1 design. Only the transceivers, switches and PLL circuit are external to the Xilinx device.

The PMC-BISERIAL-III MDS1 is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. In standard configuration, the PMC-BISERIAL-III MDS1 is a Type 1 mechanical with only low profile passive components on the back of the board, one slot wide, with 10 mm inter-board height. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and basic logic design.

A logic block within the Xilinx controls the PCI interface to the host CPU. The PMC-BISERIAL-III MDS1 design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI core decodes the address and control signals and before the “terminate with data” state is reached. Two additional clock periods account for the delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather DMA is provided for in this design. Once the physical address of the first chaining descriptor is written to the appropriate DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the I/O buffer passed to the read or write call. The next four bytes represent a long-word indicating the length of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is set to one if the I/O transfer is from the PMC-BISERIAL-III MDS1 board to host memory, and zero if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one.

The PMC-BISERIAL-III MDS1 receives Manchester encoded data MSB first in groups of 81 16-bit words with no gaps between words. With Manchester encoding there is always a data transition in the middle of a bit period, but transitions between bits are only present when the two bit values are the same. This allows the clock to be recovered from the data stream so that only a single I/O line is required to transfer data. An example of Manchester encoded data is shown in the figure below.

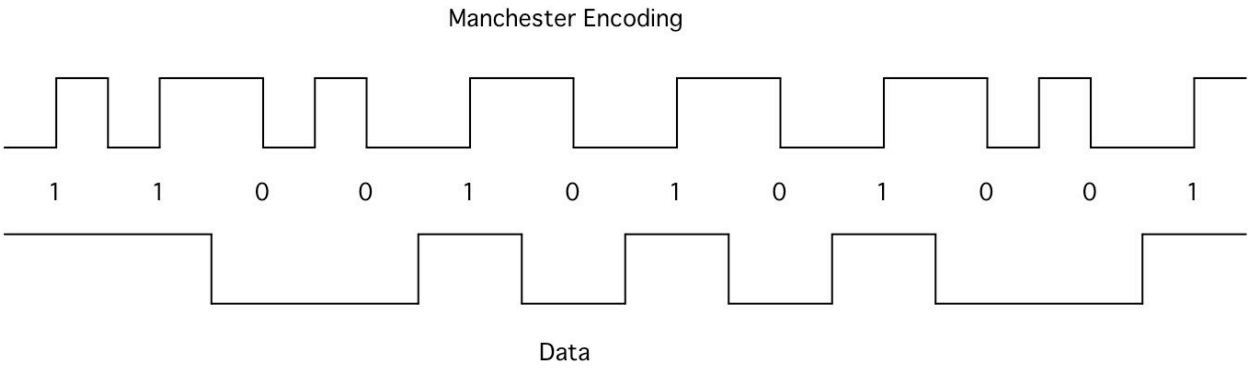


FIGURE 3 PMC-BISERIAL-III MDS1 - DATA ENCODING

Each 81 word data-block is preceded by a 16-bit sync word of alternating ones and zeros. The first data-word received is stored in the lower half of a 32-bit FIFO word and the second word is stored in the upper half. Once both halves of the FIFO word are loaded, the 32-bit word is written to the FIFO. This process continues until the 81st 16-bit word has been received. This word is stored in the lower half of the FIFO word with the upper half containing zeros. This last 32-bit word is then written to the FIFO. The unit ID code contained in bits 14 to 7 of this last I/O word is latched into an eight-bit register that can be read from bits 27 to 20 of the channel status register. After the last FIFO word is written an interrupt will occur if it has been enabled and the receiver state machine will resume looking for the next sync word.

Interrupts can also be generated when the receive data input is inactive for more than four bit periods, when an attempt is made to write to a full receive FIFO, or when the transmit state machine completes sending a block of data.

TX FIFO almost empty and RX FIFO almost full levels are programmable by writing values into the respective FIFO level registers**.** Besides generating FIFO level status, these values can also be used to cause DMA arbitration priority if enabled to do so. This process helps to prevent RX FIFO overrun when data is being received by multiple channels. If a channel has reached the FIFO almost full level, that channel will get priority in the DMA arbiter if DMA arbitration priority is enabled for that channel.

Programming

Programming the PMC-BISERIAL-III MDS1 requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BISERIAL-III MDS1 "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

Before I/O data can be sent or received, the PLL must be programmed to the desired clock configuration. The PLL is connected to the Xilinx by an I^2C serial bus. The PLL internal registers are loaded with 40 bytes of data that are derived from a .jed file generated by the CyberClock utility from Cypress semiconductor. Routines to program the PLL are included in the driver and UserApp code provided in the engineering kit for the board. http://www.dyneng.com/CyberClocks.zip

Once the PLL is programmed, in order to receive data the software is only required to enable the receiver. To transmit, the software will need to load the message into the TX FIFO, and enable the transmitter.

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the TX/RX interrupts. After an interrupt is received, new TX data can be written or RX data retrieved. An efficient loop can then be implemented to process the data. New messages can be sent or received even as the current one is in progress.

If more than one interrupt is enabled, then the software needs to read the status to see which source caused the interrupt. The status bits are latched, and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status register and write that value back to clear all the latched interrupt status bits before starting a transfer. This will insure that the interrupt status values read by the interrupt service routine came from the current transfer.

If DMA is to be used it will be necessary to acquire blocks of non-paged memory that is accessible from the PCI bus in which to store the DMA chaining descriptor list entries.

Refer to the Theory of Operation section above and the register definition section below for more information regarding the exact sequencing and interrupt definitions.

The PMC-BISERIAL-III MDS1 VendorId = 0x10EE. The CardId = 0x002B.

Address Map

Register Name	Offset	Description
PB3_MDS1_BASE	0x0000	Base control register
PB3_MDS1_PLL_WRITE	0x0000	Base control - bits 16-19 used for pll control
PB3_MDS1_PLL_READ	0x0004	Switch port bit 19 used for pll_sdat input
PB3_MDS1_USER_SWITCH	0x0004	User switch read port and Xilinx design revision
MDS1_CHAN0_CONTROL	0x0010	Channel control register
MDS1_CHAN0_STATUS	0x0014	Channel status register
MDS1_CHAN0_WR_DMA_PNTR	0x0018	Write DMA physical PCI dpr address
MDS1_CHAN0_RD_DMA_PNTR	0x001C	Read DMA physical PCI dpr address
MDS1_CHAN0_FIFO	0x0020	FIFO single word access
MDS1_CHAN0_TX_AMT_LVL	0x0024	TX almost empty level
MDS1_CHAN0_RX_AFL_LVL	0x0028	RX almost full level
MDS1_CHAN0_TX_FIFO_COUNT	0x002C	TX FIFO count
MDS1_CHAN0_RX_FIFO_COUNT	0x0030	RX FIFO count
MDS1_CHAN1_CONTROL	0x0034	Channel control register
MDS1_CHAN1_STATUS	0x0038	Channel status register
MDS1_CHAN1_WR_DMA_PNTR	0x003C	Write DMA physical PCI dpr address
MDS1_CHAN1_RD_DMA_PNTR	0x0040	Read DMA physical PCI dpr address
MDS1_CHAN1_FIFO	0x0044	FIFO single word access
MDS1_CHAN1_TX_AMT_LVL	0x0048	TX almost empty level
MDS1_CHAN1_RX_AFL_LVL	0x004C	RX almost full level
MDS1_CHAN1_TX_FIFO_COUNT	0x0050	TX FIFO count
MDS1_CHAN1_RX_FIFO_COUNT	0x0054	RX FIFO count
MDS1_CHAN2_CONTROL	0x0058	Channel control register
MDS1_CHAN2_STATUS	0x005C	Channel status register
MDS1_CHAN2_WR_DMA_PNTR	0x0060	Write DMA physical PCI dpr address
MDS1_CHAN2_RD_DMA_PNTR	0x0064	Read DMA physical PCI dpr address
MDS1_CHAN2_FIFO	0x0068	FIFO single word access
MDS1_CHAN2_TX_AMT_LVL	0x006C	TX almost empty level
MDS1_CHAN2_RX_AFL_LVL	0x0070	RX almost full level
MDS1_CHAN2_TX_FIFO_COUNT	0x0074	TX FIFO count
MDS1_CHAN2_RX_FIFO_COUNT	0x0078	RX FIFO count
MDS1_CHAN3_CONTROL	0x007C	Channel control register
MDS1_CHAN3_STATUS	0x0080	Channel status register
MDS1_CHAN3_WR_DMA_PNTR	0x0084	Write DMA physical PCI dpr address
MDS1_CHAN3_RD_DMA_PNTR	0x0088	Read DMA physical PCI dpr address
MDS1_CHAN3_FIFO	0x008C	FIFO single word access
MDS1_CHAN3_TX_AMT_LVL	0x0090	TX almost empty level
MDS1_CHAN3_RX_AFL_LVL	0x0094	RX almost full level
MDS1_CHAN3_TX_FIFO_COUNT	0x0098	TX FIFO count
MDS1_CHAN3_RX_FIFO_COUNT	0x009C	RX FIFO count

FIGURE 4 PMC-BISERIAL-III MDS1 XILINX ADDRESS MAP

Register Definitions

PB3_MDS1_BASE

[0x0000] Base Control Register (read/write)

Base Control Register

Data Bit	Description
31-20	Spare
19	PLL Sdata Output
18	PLL S2 Output
17	PLL Sclk Output
16	PLL Enable
15-0	Spare

FIGURE 5 PMC-BISERIAL-III MDS1 BASE CONTROL REGISTER

All bits are active high and are reset on power-up or reset command, except PLL enable, which defaults to enabled (high) on power-up or reset.

PLL Enable: When this bit is set to a one, the signals used to program and read the PLL are enabled.

PLL Sclk/Sdata Output: These signals are used to program the PLL over the I^2C serial interface. Sclk is always an output whereas Sdata is bi-directional. This register is where the Sdata output value is specified. When Sdata is an input it is read from the User Switch Port.

PLL S2 Output: This is an additional control line to the PLL that can be used to select additional pre-programmed frequencies.

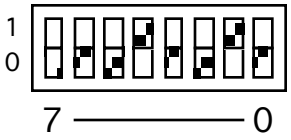
PB3_MDS1_USER_SWITCH

[0x0004] User Switch Port (read only)

Dip-Switch Port	
Data Bit	**Description**
31-20	Spare
19	PLL Sdata Input
18-16	Spare
15-8	Xilinx Design Revision Number
7-0	Switch Setting

FIGURE 6 PMC-BISERIAL-III MDS1 USER SWITCH PORT

Switch Setting: The user switch is read through this port. The bits are read as the lowest byte in the port. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



Xilinx Design Revision Number: The value of the second byte of this port is the rev. number of the Xilinx design (currently 0x02 - rev. B).

PLL Sdata Input: The PLL_sdata bi-directional line is read using this bit. This line is used to read the register contents of the PLL.

MDS1_CHAN0-3_CONTROL

[0x0010, 0x0034, 0x0058, 0x007C] Channel Control Register (read/write)

Base Control Register

Data Bit	Description
31-16	Spare
15	RX DMA Priority Arbitration Enable
14	TX DMA Priority Arbitration Enable
13	RX Inactive Interrupt Enable
12	TX and RX Data Invert
11	RX Termination Enable
10	RX FIFO Overflow Interrupt Enable
9	RX Interrupt Enable
8	TX Interrupt Enable
7	RX Enable
6	TX Enable
5	Force Interrupt
4	Master Interrupt Enable
3	Read DMA Interrupt Enable
2	Write DMA Interrupt Enable
1	FIFO Bypass Enable
0	FIFO Reset

FIGURE 7 PMC-BISERIAL-III MDS1 CHANNEL CONTROL REGISTER

FIFO Reset: When this bit is set to a one, the transmit and receive FIFOs will be reset. When this bit is zero, normal FIFO operation is enabled.

FIFO Bypass Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without using the I/O. When this bit is zero, normal operation is enabled.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA writes and reads respectively. The DMA interrupts are not affected by the Master Interrupt Enable.

Master Interrupt Enable: When this bit is set to a one, all enabled interrupts (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one, a system interrupt will occur provided the master interrupt enable is set. This is useful for interrupt testing.

TX Enable: When this bit is set to a one, I/O data will be transmitted provided at least 41 words are loaded into the TX FIFO and the PLL has been configured. When this bit is a zero the transmitter is disabled.

RX Enable: When this bit is set to a one, the receiver is enabled and will start to look for received serial data beginning with the sync word. When this bit is zero, the receiver is disabled.

TX Interrupt Enable: When this bit is set to a one, the transmit interrupt is enabled. A transmit interrupt will be asserted when a data-block has been completely sent, provided the master interrupt enable is asserted. When this bit is zero, the transmit interrupt is disabled.

RX Interrupt Enable: When this bit is set to a one, the receive interrupt is enabled. A receive interrupt will be asserted, provided the master interrupt is enabled when at least one data-block has been received. When this bit is zero, the receive interrupt is disabled.

RX FIFO Overflow Interrupt Enable: When this bit is set to a one, the receive FIFO overflow interrupt is enabled. An interrupt will be asserted, provided the master interrupt is enabled when an attempt is made to write to a full receive FIFO. When this bit is zero, the receive FIFO overflow interrupt is disabled.

RX Termination Enable: When this bit is set to a one, the 100 Ω receiver I/O shunt termination is enabled. This termination is used to reduce noise on the I/O line. If more than one receiver is being driven by the same source, be careful not to enable more than one termination as this could excessively attenuate the signal. When this bit is zero, the termination is disabled.

TX & RX Data Invert: When this bit is set to a one, the data sent from the transmitter and the data input to the receiver are inverted. This is the normal operational mode for the MDS1 design as determined by connection to the target data source. See figure 3 for the correct code interpretation with this bit set.

RX Inactive Interrupt Enable: When this bit is set to a one, the receive data inactive interrupt is enabled. An interrupt will be asserted, provided the master interrupt is enabled when the receiver is enabled and the input data line becomes inactive for at least four bit-periods. When this bit is zero, the receive data inactive interrupt is disabled.

TX/RX DMA Priority Arbitration Enable: When this bit is set to a one, the corresponding DMA channel will have priority if it is near the limit of its FIFO (almost empty for the TX

or almost full for the RX). These limits are derived from the programmable counts in the MDS1_CHAN0-3_TX_AMT_LVL and MDS1_CHAN0-3_RX_AFL_LVL registers.

MDS1_CHAN0-3_STATUS

[0x0014, 0x0038, 0x005C, 0x0080] Channel Status Read/Latch Write Port

Status Register

Data Bit	Description
31	Channel Interrupt Active
30-28	Spare
27-20	Unit ID
19-17	Spare
16	User Interrupt Condition Occurred
15	Read DMA Interrupt Occurred
14	Write DMA Interrupt Occurred
13	Read DMA Error Occurred
12	Write DMA Error Occurred
11	RX Inactivity Occurred
10	TX Interrupt Occurred
9	RX Interrupt Occurred
8	RX FIFO Overflow Occurred
7	Receive Data Valid
6	Receive FIFO Full
5	Receive FIFO Almost Full
4	Receive FIFO Empty
3	Spare
2	Transmit FIFO Full
1	Transmit FIFO Almost Empty
0	Transmit FIFO Empty

FIGURE 8 PMC-BISERIAL-III MDS1 CHANNEL STATUS PORT

Transmit FIFO Empty: When a one is read, the transmit data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Transmit FIFO Almost Empty: When a one is read, the number of data words in the transmit data FIFO is less than or equal to the value written to the PB3_MDS1_TX_AMT_LVL register; when a zero is read, the level is more than that value.

Transmit FIFO Full: When a one is read, the transmit data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive FIFO Empty: When a one is read, the receive data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data words in the receive data FIFO is greater or equal to the value written to the PB3_MDS1_RX_AFL_LVL register; when a zero is read, the level is less than that value.

Receive FIFO Full: When a one is read, the receive data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive Data Valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO is empty, because as soon as the first four words are written into the FIFO, they are read out to be ready for a PCI read DMA or single word access. When this bit is a zero, it indicates that there is no valid receive data.

RX FIFO Overflow Occurred: When a one is read, it indicates that an attempt has been made to write data to a full receive data FIFO. A zero indicates that no overflow condition has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

RX Interrupt Occurred: When a one is read, it indicates that the receive state-machine has received at least one data-block. A zero indicates that a data-block has not been received. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

TX Interrupt Occurred: When a one is read, it indicates that the transmit state-machine sent at least one data-block. A zero indicates that a data-block has not been sent. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

RX Inactivity Occurred: When a one is read, it indicates that the receive state-machine is enabled and has received a sync word and then the data input became inactive for a minimum of four bit periods. A zero indicates that this condition has not occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Write DMA Error Occurred: When a one is read, a write DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is a one. A zero indicates that no write DMA error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Read DMA Error Occurred: When a one is read, a read DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is a zero. A zero indicates that no read DMA error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.
Write DMA Interrupt Occurred: When a one is read, a write DMA interrupt is latched. This indicates that the scatter-gather list for the current write DMA has completed, but the associated interrupt has yet to be completely processed. A zero indicates that no write DMA interrupt is pending.

Read DMA Interrupt Occurred: When a one is read, it indicates that a read DMA interrupt is latched. This indicates that the scatter-gather list for the current read DMA has completed, but the associated interrupt has yet to be completely processed. A zero indicates that no read DMA interrupt is pending.

User Interrupt Condition Occurred: When a one is read, it indicates that an enabled user interrupt condition has occurred. These conditions include the TX and RX interrupts as well as the RX FIFO overflow and RX data inactive interrupts. Also the Force Interrupt bit will cause this bit to be asserted. A system interrupt will occur if the Master Interrupt Enable is set. A zero indicates that no enabled local interrupt condition is active.

Unit ID: When a data-block is received the last 16-bit word contains the unit ID in bits 14 to 7. The receive state-machine will extract this value and store it in a latch. The unit ID value can then be read in this field.

Channel Interrupt Active: When a one is read, it indicates that a system interrupt is asserted caused by an enabled channel interrupt condition. A zero indicates that no system interrupt is pending from an enabled channel interrupt condition

MDS1_CHAN0-3_WR_DMA_PNTR

[0x0018, 0x003C, 0x0060, 0x0084] Write DMA Pointer (write only)

DMA Pointer Address Register	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 9 PMC-BISERIAL-III MDS1 WRITE DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather write DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer containing the data to write to the device, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

Note: Writing a zero to this port will abort a write DMA in progress.

MDS1_CHAN0-3_RD_DMA_PNTR

[0x001C, 0x0040, 0x0064, 0x0088] Read DMA Pointer (write only)

DMA Pointer Address Register	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 10 PMC-BISERIAL-III MDS1 READ DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather read DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer where the data from the device will be stored, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

Note: Writing a zero to this port will abort a read DMA in progress.

MDS1_CHAN0-3_FIFO

[0x0020, 0x0044, 0x0068, 0x008C] Write TX/Read RX FIFO Port

RX and TX FIFO Port	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 11 PMC-BISERIAL-III MDS1 RX/TX FIFO PORT

This port is used to make single-word accesses in to the TX and out of the RX FIFOs.

MDS1_CHAN0-3_TX_AMT_LVL

[0x0024, 0x0048, 0x006C, 0x0090] TX almost-empty level (read/write)

TX Almost-Empty Level Register	
Data Bit	**Description**
31-16	Spare
15-0	TX FIFO almost-empty level

FIGURE 12 PMC-BISERIAL-III MDS1 TX ALMOST EMPTY LEVEL REGISTER

This read/write port accesses the transmitter almost-empty level register. When the number of data words in the transmit data FIFO is equal or less than this value, the almost-empty status bit is set.

MDS1_CHAN0-3_RX_AFL_LVL

[0x0028, 0x004C, 0x0070, 0x0094] RX almost-full level (read/write)

RX Almost-Full Level Register	
Data Bit	**Description**
31-16	Spare
15-0	RX FIFO almost-full level

FIGURE 13 PMC-BISERIAL-III MDS1 RX ALMOST FULL LEVEL REGISTER

This read/write port accesses the receiver almost-full level register. When the number of data words in the receive data FIFO is equal or greater than this value, the almost-full status bit is set.

MDS1_CHAN0-3_TX_FIFO_COUNT

[0x002C, 0x0050, 0x0074, 0x0098] TX FIFO data count (read only)

TX FIFO Data Count Port

Data Bit	Description
31-12	Spare
11-0	TX data words stored

FIGURE 14 PMC-BISERIAL-III MDS1 TX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the transmit FIFO and data holding register (currently a maximum of 0x401).

MDS1_CHAN0-3_RX_FIFO_COUNT

[0x0030, 0x0054, 0x0078, 0x009C] RX FIFO data count (read only)

RX FIFO Data Count Port

Data Bit	Description
31-12	Spare
11-0	RX data words stored

FIGURE 15 PMC-BISERIAL-III MDS1 RX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the receive FIFO and data pipeline (currently a maximum of 0x404).

Loop-back

The Engineering kit has reference software, which includes external loop-back tests. The PMC-BISERIAL-III MDS1 has a 68 pin SCSI II front panel connector. The tests require an external cable with the following pins connected.

Signal	From	To	Signal
TX0 DATA+	pin 1	pin 17	RX0 DATA+
TX0 DATA-	pin 35	pin 51	RX0 DATA-
TX1 DATA+	pin 2	pin 18	RX1 DATA+
TX1 DATA-	pin 36	pin 52	RX1 DATA-
TX2 DATA+	pin 3	pin 19	RX2 DATA+
TX2 DATA -	pin 37	pin 53	RX2 DATA-
TX3 DATA+	pin 4	pin 20	RX3 DATA+
TX3 DATA-	pin 38	pin 54	RX3 DATA-

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BISERIAL-III MDS1. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification but not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 16 PMC-BISERIAL-III MDS1 PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BISERIAL-III MDS1. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification but not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 17 PMC-BISERIAL-III MDS1 PN2 INTERFACE

BiSerial III Front Panel I/O Pin Assignment

The figure below gives the pin assignments for the PMC Module I/O Interface on the **PMC-BiSerial-III MDS1.** For a customized version, or other options, contact Dynamic Engineering.

IO_0p (TX0 DATA+)	IO_0m (TX0 DATA-)	1	35
IO_1p (TX1 DATA+)	IO_1m (TX1 DATA-)	2	36
IO_2p (TX2 DATA+)	IO_2m (TX2 DATA-)	3	37
IO_3p (TX3 DATA+)	IO_3m (TX3 DATA-)	4	38
IO_4p	IO_4m	5	39
IO_5p	IO_5m	6	40
IO_6p	IO_6m	7	41
IO_7p	IO_7m	8	42
IO_8p	IO_8m	9	43
IO_9p	IO_9m	10	44
IO_10p	IO_10m	11	45
IO_11p	IO_11m	12	46
IO_12p	IO_12m	13	47
IO_13p	IO_13m	14	48
IO_14p	IO_14m	15	49
IO_15p	IO_15m	16	50
IO_16p (RX0 DATA+)	IO_16m (RX0 DATA-)	17	51
IO_17p (RX1 DATA+)	IO_17m (RX1 DATA-)	18	52
IO_18p (RX2 DATA+)	IO_18m (RX2 DATA-)	19	53
IO_19p (RX3 DATA+)	IO_19m (RX3 DATA-)	20	54
IO_20p	IO_20m	21	55
IO_21p	IO_21m	22	56
IO_22p	IO_22m	23	57
IO_23p	IO_23m	24	58
IO_24p	IO_24m	25	59
IO_25p	IO_25m	26	60
IO_26p	IO_26m	27	61
IO_27p	IO_27m	28	62
IO_28p	IO_28m	29	63
IO_29p	IO_29m	30	64
IO_30p	IO_30m	31	65
IO_31p	IO_31m	32	66
IO_32p	IO_32m	33	67
IO_33p	IO_33m	34	68

FIGURE 18 PMC-BISERIAL-III MDS1 FRONT PANEL INTERFACE

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling the PMC-BISERIAL-III MDS1. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. Look quickly, if the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. We use PCIView.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BISERIAL-III MDS1 is constructed out of 0.062-inch thick FR4 material.

Through-hole and surface-mount components are used. The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-BISERIAL-III MDS1 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, then forced-air cooling is recommended. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
150 DuBois, Suite C
Santa Cruz, CA 95060
(831) 457-8891 Fax (831) 457-4793
support@dyneng.com

Specifications

Host Interface:	[PMC] PCI Mezzanine Card – 32-bit, 33 MHz
Serial Interfaces:	Eight serial interfaces (four in and four out). 16-bit word size, MSB first, Manchester encoded data in blocks of 81 words with a preceding sync word
TX Bit-rates generated:	192 Kbits/second for TX and RX serial channels, 2x and 8x clock references supplied by the on-board PLL
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory map)
Wait States:	One for all addresses
Interrupt:	TX data-block sent, RX data-block received, RX FIFO overflow and RX data inactive
DMA:	Scatter/Gather DMA Support implemented
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module
Construction:	FR4 Multi-Layer Printed Circuit, Through-Hole and Surface-Mount Components
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V
Temperature range	Standard (0 to +70) Extended Temperature available (-40 to +85)

Order Information

PMC-BISERIAL-III MDS1	PMC Module with 4 serial channels, two RS-485 I/O per channel (one in and one out), Manchester encoded data
Eng Kit PMC-BISERIAL-III MDS1	HDEterm68 - 68 position screw terminal adapter http://www.dyneng.com/HDEterm68.html HDEcabl68 - 68 I/O twisted pair cable http://www.dyneng.com/HDEcabl68.html Technical Documentation, 1. PMC-BiSerial-III Schematic 2. PMC-BISERIAL-III MDS1 Driver software and user application. Data sheet reprints are available from the manufacturer's web site

***Note**: The Engineering Kit is strongly recommended for first time* **PMC-BiSerial**-III *purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. The revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.