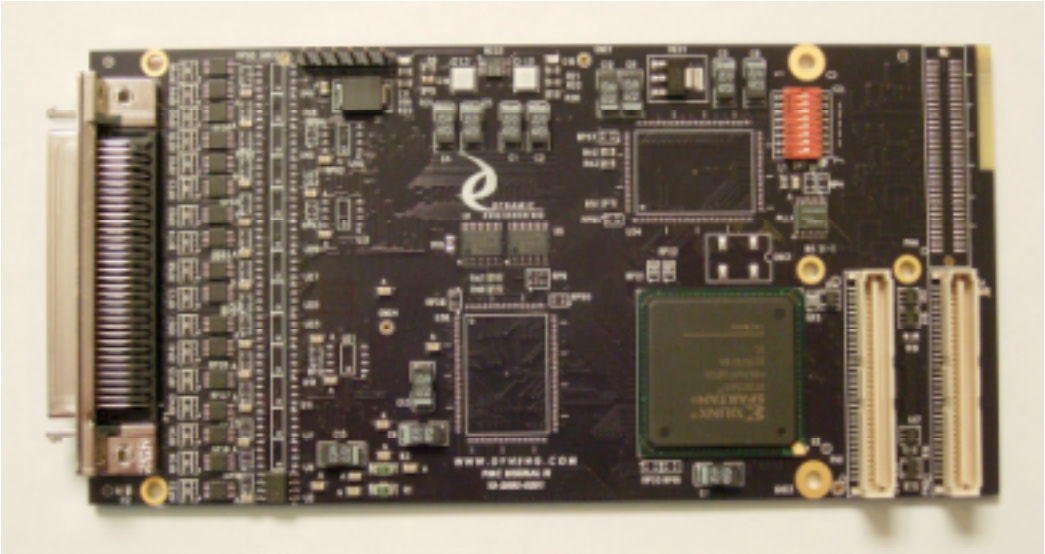
DYNAMIC ENGINEERING
435 Park Dr., Ben Lomond, Calif. 95005
831-336-8891 **Fax** 831-336-3840
http://www.dyneng.com
sales@dyneng.com
Est. 1988

User Manual

PMC-BiSerial-III-LM5

Octal Bi-directional Serial Interface PMC Module



Revision A
Corresponding Hardware: Revision B/C
10-2005-0502/3
Corresponding Firmware: Revision A

PMC-BiSerial-III-LM5
Octal Bi-Directional Serial
Data Interface
PMC Module

Dynamic Engineering
435 Park Drive
Ben Lomond, CA 95005
831-336-8891
831-336-3840 FAX

Manual Revision A. Revised October 27, 2006

Table of Contents

List of Figures

Product Description

The PMC-BiSerial-III-LM5 is part of the PMC Module family of modular I/O components by Dynamic Engineering. The PMC-BiSerial-III is capable of providing multiple serial protocols. The LM5 protocol implemented provides eight transmit and receive channels each consisting of LVDS clock, data, and strobe The data path is two bits wide. The transmitter operates at 40 MHz for an effective 80Mhz transfer rate.

Other custom interfaces are available. We will redesign the state machines and create a custom interface protocol. That protocol will then be offered as a “standard” special order product. Please see our web page for current protocols offered. Please contact Dynamic Engineering with your custom application.

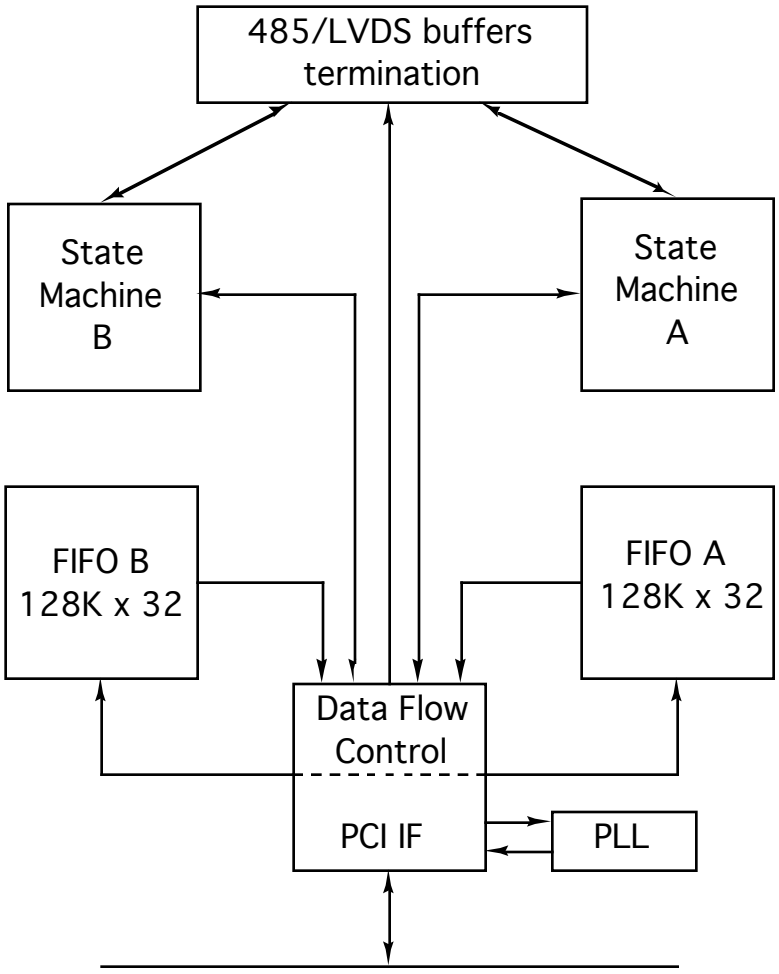


FIGURE 1 PMC-BISERIAL-III BLOCK DIAGRAM

The standard configuration shown in Figure 1 makes use of two external [to the Xilinx] FIFOs. The FIFOs can be as large as 128K deep x 32 bits wide. Most designs do not

require so much memory, and are more efficiently implemented using FIFOs internal to the Xilinx FPGA.

The LM5 implementation has 16 1K by 32-bit FIFOs using the Xilinx internal block RAM, one for each transmitter and one for each receiver. Data is transmitted MSB first in a continuous bit stream as long as the transmitter is enabled and data is present in the TX FIFO.

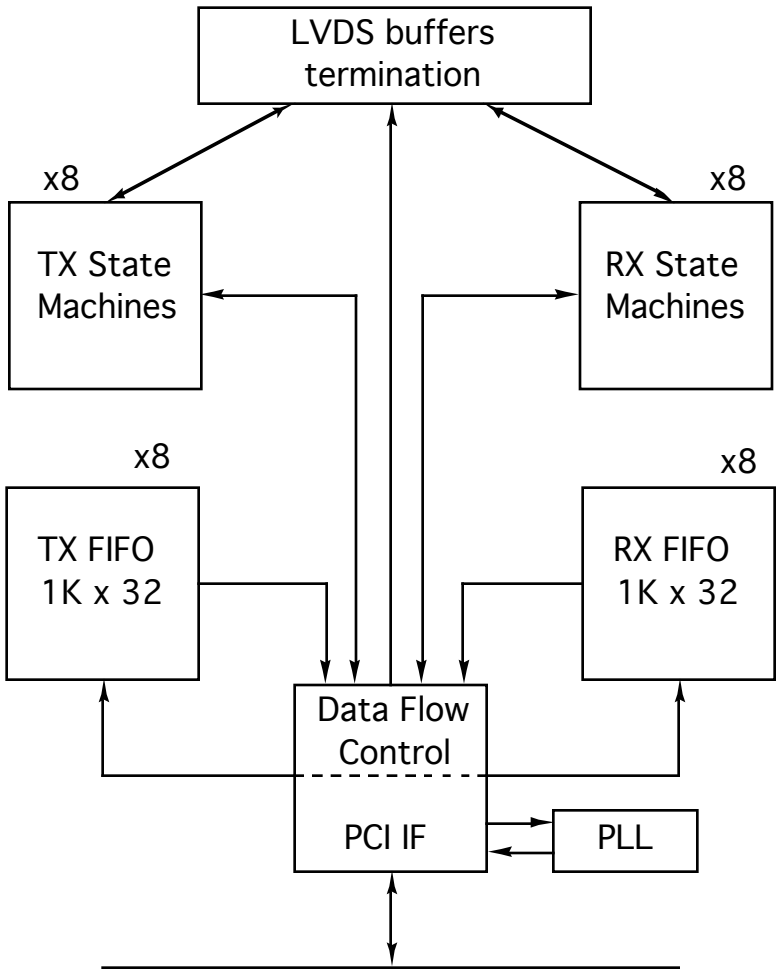


FIGURE 2 PMC-BISERIAL-III-LM5 BLOCK DIAGRAM

The data rate is set to 40 MHz based on a reference oscillator. The on-board PLL has not been implemented for this design. If you need an alternate frequency please contact Dynamic Engineering

Thirty-four differential I/O are provided at the front bezel for the serial signals. The drivers and receivers conform to the LVDS specification. The LVDS input signals are selectively terminated with 100Ω. The termination resistors are in two-element packages to allow flexible termination options for custom formats and protocols. Optional pullup/pulldown resistor packs can also be installed to provide a logic '1' on un-driven lines.

This design uses 32 of the I/O lines. Each transmitter and receiver has a clock, two data, and a strobe. Each channel has one transmitter and one receiver that are used in as half duplex. Software controls the transmit or receive functionality.

The PMC-BiSerial-III-LM5 conforms to the PMC and CMC draft standards. This guarantees compatibility with multiple PMC Carrier boards. Because the PMC may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one PMC Carrier board, while final system implementation uses a different one.

The PMC-BiSerial-III-LM5 uses a 10 mm inter-board spacing for the front panel, standoffs, and PMC connectors. The 10 mm height is the "standard" height and will work in most systems with most carriers. If your carrier has non-standard connectors (height) to mate with the PMC-BiSerial-III-LM5, please let us know. We may be able to do a special build with a different height connector to compensate.

Various interrupts are supported by the PMC BiSerial-III-LM5. An interrupt can be configured to occur at the end of a transmitted message. An interrupt can be set at the end of a received data-word. FIFO level interrupts and DMA complete interrupts are also supported. All interrupts are individually maskable, and a master interrupt enable is also provided to disable all interrupts simultaneously. The current status is available making it possible to operate in a polled mode when interrupts are disabled. All configuration registers support read and write operations for maximum software convenience. All addresses are long word (32-bit) aligned.

Theory of Operation

The PMC-BiSerial-III-LM5 features a Xilinx FPGA. The FPGA contains all of the registers, FIFOs and protocol controlling elements of the PMC-BiSerial-III-LM5 design. Only the transceivers, switches and PLL circuit are external to the Xilinx device.

The PMC-BiSerial-III-LM5 is a part of the PMC Module family of modular I/O products. It meets the PMC and CMC draft Standards. In standard configuration, the PMC-BiSerial-III-LM5 is a Type 1 mechanical with only low profile passive components on the back of the board, one slot wide, with 10 mm inter-board height. Contact Dynamic Engineering for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and basic logic design.

A logic block within the Xilinx controls the PCI interface to the host CPU. The PMC-BiSerial-III-LM5 design requires one wait state for read or writes cycles to any address. The wait states refer to the number of clocks after the PCI core decode before the “terminate with data” state is reached. Two additional clock periods account for the 1 clock delay to decode the signals from the PCI bus and to convert the terminate-with-data state into the TRDY signal.

Scatter-gather DMA is provided for in this design. Once the physical address of the first chaining descriptor is written to the appropriate DMA pointer register, the interface will read a 12-byte block from this location. The first four bytes comprise a long-word indicating the physical address of the first block of the IO buffer passed to the read or write call. The next four bytes represent a long-word indicating the length of that block. The final four bytes are a long-word indicating the physical address of the next chaining descriptor along with two flag bits, in bit position 0 and 1. Bit zero is set to one if this descriptor is the last in the chain. Bit one is set to one if the IO transfer is from the PMC-BiSerial-III-LM5 board to host memory, and zero if the transfer is from memory to the board. These bits are then replaced with zeros to determine the address of the next descriptor, if there is one.

The PMC-BiSerial-III-LM5 sends data MSB first. The clock is always driven. The timing is shown in the figure below.

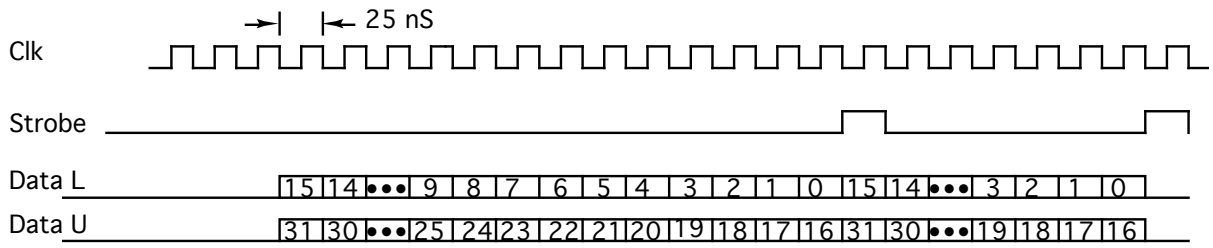


FIGURE 3 PMC BISERIAL-III-LM5 TIMING DIAGRAM

Currently the TX data rate is set to 40 MHz. The DMA FIFO IO side clock reference is 66 MHz. Alternate frequencies up to 66 MHz. can be implemented with little change to the current design. In many cases just changing out the oscillator will be all that is required. The on board PLL can be implemented if programmable rates are needed for your design.

Data is sent MSB first in a two bit stream so 16 clocks are required to send the 32 bit word. The strobe is set on the clock following the 16th bit to allow a simple shift register followed by a register to be used to capture data on the receive side. The clock is free running and the strobe captures the last 32 bits received allowing for any number of wait-states on the transmitter side to be implemented. If the strobe is activated as shown above the previous data is captured while the next word is starting to shift in for a pipelined operation with no overhead.

The transmitter will continue to send data as long as it is enabled and there is data in the FIFO. When the FIFO becomes empty, a TX interrupt pulse is generated by the state-machine. The pulse can be masked to allow polled operation.

The receiver clocks data into a 32-bit shift register. When 32 bits have been received, the data word is written to the RX FIFO and the process continues. If the receive interrupt is enabled, an interrupt pulse will be generated for each word received.

Interrupts can also be triggered by the completion of a read or write DMA to facilitate data transfer efficiency.

There are 8 transmitters coupled with 8 receivers. Each channel is programmable for transmit or receive mode. The mode can be switched on the fly. The clock, data, and strobe switch from output to input or vice-versa. It is best to do the switch when the state-machine is “at rest” having completed a transmission before switching to reception. The completion interrupt can be used to “know” when the transmitter has

returned to the Idle state. The receiver is designed to operate with mixed rate and stopped clock situations. The enables for the receiver and transmitter are independent to allow both to be enabled or disabled. When a channel is not being used it can be completely disabled and the IO definition set to receive.

Each of the 16 channels [8 TX and 8 RX] has a separate DMA capability. The channels each have independent counter / pointer logic to allow multiple DMA transfers to be processed in parallel. The DMA engines are regulated with an internal arbiter to determine which channel gets to use the PCI bus at a particular time. With the separate channels large transfers can be programmed and run autonomously with the interrupt at the end of the transfer to indicate completion. Much lower interrupt handing requirements means much better throughput and less overhead on the system CPU.

The arbitration and channel operation are completely automatic.

Programming

Programming the PMC-BiSerial-III-LM5 requires only the ability to read and write data from the host. The base address is determined during system configuration of the PCI bus. The base address refers to the first user address for the slot in which the PMC is installed.

Depending on the software environment it may be necessary to set-up the system software with the PMC-BiSerial-III-LM5 "registration" data. For example in WindowsNT there is a system registry, which is used to identify the resident hardware.

In order to receive data the software is only required to enable the receiver. To transmit, the software will need to load the message into the TX FIFO, select the clock reference and enable the transmitter.

The interrupt service routine should be loaded and the interrupt mask set. The interrupt service routine can be configured to respond to the FIFO level interrupts, the TX/RX interrupts, and/or the DMA completion interrupts. After an interrupt is received, new TX data can be written or RX data retrieved. An efficient loop can then be implemented to process the data. New messages can be sent or received even as the current one is in process.

If more than one interrupt is enabled, then the software needs to read the status to see which source caused the interrupt. The status bits are latched, and are explicitly cleared by writing a one to the corresponding bit. It is a good idea to read the status register and write that value back to clear all the latched interrupt status bits before starting a transfer. This will insure that the interrupt status values read by the interrupt service routine came from the current transfer.

If DMA is to be used it will be necessary to acquire blocks of non-paged memory that is accessible from the PCI bus in which to store the chaining descriptor list entries.

Refer to the Theory of Operation section above and the register definition section below for more information regarding the exact sequencing and interrupt definitions.

Address Map

Register Name	Offset	Description
BIS3_IO_BASE	0x0000	// 0 Base control register
BIS3_IO_ID	0x0004	// 1 User switch and FLASH revision read only port
BIS3_IO_DIR	0x000C	// 3 PMC BiSerial3 Direction Register 31 - 0 with read-back
BIS3_IO_DATA	0x0010	// 4 PMC BiSerial3 Data Register 31 - 0 with direct read-back from IO
BIS3_IO_DATA_REG	0x0014	// 5 PMC BiSerial3 read only register DATA path
BIS3_IO_MUX	0x0018	// 6 PMC BiSerial3 MUX Register 31 - 0 with read-back
BIS3_IO_TERM	0x001C	// 7 PMC BiSerial3 Termination Register 31 - 0 with read-back
PMC_BIS3_BASE0	0x0078	// 30 base register for channel 0 DMA control
PMC_BIS3_STAT0	0x007C	// 31 Interrupt status channel 0
PMC_BIS3_WR_DMA_PNTR0	0x0080	// 32 Burst In 0
PMC_BIS3_RD_DMA_PNTR0	0x0084	// 33 Burst Out 0
PMC_BIS3_FIFORW0	0x0088	// 34 Channel 0 DMA single write / read FIFO
PMC_BIS3_TX_AMT_LVL0	0x008C	// 35 TX Almost Empty Count 0
PMC_BIS3_RX_AFL_LVL0	0x0090	// 36 RX Almost Full Count 0
PMC_BIS3_TX_FIFO_COUNT0	0x0094	// 37 TX FIFO word count 0
PMC_BIS3_RX_FIFO_COUNT0	0x0098	// 38 RX FIFO word count 0
PMC_BIS3_FIFORW0	0x009C	// 39 Spare
PMC_BIS3_BASE1	0x00A0	// 40 base register for channel 1 DMA control
PMC_BIS3_STAT1	0x00A4	// 41 Interrupt status channel 1
PMC_BIS3_WR_DMA_PNTR1	0x00A8	// 42 Burst In 1
PMC_BIS3_RD_DMA_PNTR1	0x00AC	// 43 Burst Out 1
PMC_BIS3_FIFORW1	0x00B0	// 44 Channel 1 DMA single write / read FIFO
PMC_BIS3_TX_AMT_LVL1	0x00B4	// 45 TX Almost Empty Count 1
PMC_BIS3_RX_AFL_LVL1	0x00B8	// 46 RX Almost Full Count 1
PMC_BIS3_TX_FIFO_COUNT1	0x00BC	// 47 TX FIFO word count 1
PMC_BIS3_RX_FIFO_COUNT1	0x00C0	// 48 RX FIFO word count 1
PMC_BIS3_FIFORW1	0x00C4	// 49 Spare
PMC_BIS3_BASE2	0x00C8	// 50 base register for channel 2 DMA control
PMC_BIS3_STAT2	0x00CC	// 51 Interrupt status channel 2
PMC_BIS3_WR_DMA_PNTR2	0x00D0	// 52 Burst In 2
PMC_BIS3_RD_DMA_PNTR2	0x00D4	// 53 Burst Out 2
PMC_BIS3_FIFORW2	0x00D8	// 54 Channel 2 DMA single write / read FIFO
PMC_BIS3_TX_AMT_LVL2	0x00DC	// 55 TX Almost Empty Count 2
PMC_BIS3_RX_AFL_LVL2	0x00E0	// 56 RX Almost Full Count 2
PMC_BIS3_TX_FIFO_COUNT2	0x00E4	// 57 TX FIFO word count 2
PMC_BIS3_RX_FIFO_COUNT2	0x00E8	// 58 RX FIFO word count 2
PMC_BIS3_FIFORW2	0x00EC	// 59 Spare
PMC_BIS3_BASE3	0x00F0	// 60 base register for channel 3 DMA control
PMC_BIS3_STAT3	0x00F4	// 61 Interrupt status channel 3
PMC_BIS3_WR_DMA_PNTR3	0x00F8	// 62 Burst In 3
PMC_BIS3_RD_DMA_PNTR3	0x00FC	// 63 Burst Out 3
PMC_BIS3_FIFORW3	0x0100	// 64 Channel 3 DMA single write / read FIFO
PMC_BIS3_TX_AMT_LVL3	0x0104	// 65 TX Almost Empty Count 3
PMC_BIS3_RX_AFL_LVL3	0x0108	// 66 RX Almost Full Count 3
PMC_BIS3_TX_FIFO_COUNT3	0x010C	// 67 TX FIFO word count 3
PMC_BIS3_RX_FIFO_COUNT3	0x0110	// 68 RX FIFO word count 3
PMC_BIS3_FIFORW3	0x0114	// 69 Spare

```
PMC_BIS3_BASE4              0x0118  // 70 base register for channel 4 DMA control
PMC_BIS3_STAT4              0x011C  // 71 Interrupt status channel 4
PMC_BIS3_WR_DMA_PNTR4       0x0120  // 72 Burst In  4
PMC_BIS3_RD_DMA_PNTR4       0x0124  // 73 Burst Out 4
PMC_BIS3_FIFORW4            0x0128  // 74 Channel 4 DMA single write / read FIFO
PMC_BIS3_TX_AMT_LVL4        0x012C  // 75 TX Almost Empty Count 4
PMC_BIS3_RX_AFL_LVL4        0x0130  // 76 RX Almost Full Count 4
PMC_BIS3_TX_FIFO_COUNT4     0x0134  // 77 TX FIFO word count 4
PMC_BIS3_RX_FIFO_COUNT4     0x0138  // 78 RX FIFO word count 4
PMC_BIS3_FIFORW4            0x013C  // 79 Spare

PMC_BIS3_BASE5              0x0140  // 80 base register for channel 5 DMA control
PMC_BIS3_STAT5              0x0144  // 81 Interrupt status channel 5
PMC_BIS3_WR_DMA_PNTR5       0x0148  // 82 Burst In  5
PMC_BIS3_RD_DMA_PNTR5       0x014C  // 83 Burst Out 5
PMC_BIS3_FIFORW5            0x0150  // 84 Channel 5 DMA single write / read FIFO
PMC_BIS3_TX_AMT_LVL5        0x0154  // 85 TX Almost Empty Count 5
PMC_BIS3_RX_AFL_LVL5        0x0158  // 86 RX Almost Full Count 5
PMC_BIS3_TX_FIFO_COUNT5     0x015C  // 87 TX FIFO word count 5
PMC_BIS3_RX_FIFO_COUNT5     0x0160  // 88 RX FIFO word count 5
PMC_BIS3_FIFORW5            0x0164  // 89 Spare

PMC_BIS3_BASE6              0x0168  // 90 base register for channel 6 DMA control
PMC_BIS3_STAT6              0x016C  // 91 Interrupt status channel 6
PMC_BIS3_WR_DMA_PNTR6       0x0170  // 92 Burst In  6
PMC_BIS3_RD_DMA_PNTR6       0x0174  // 93 Burst Out 6
PMC_BIS3_FIFORW6            0x0178  // 94 Channel 6 DMA single write / read FIFO
PMC_BIS3_TX_AMT_LVL6        0x017C  // 95 TX Almost Empty Count 6
PMC_BIS3_RX_AFL_LVL6        0x0180  // 96 RX Almost Full Count 6
PMC_BIS3_TX_FIFO_COUNT6     0x0184  // 97 TX FIFO word count 6
PMC_BIS3_RX_FIFO_COUNT6     0x0188  // 98 RX FIFO word count 6
PMC_BIS3_FIFORW6            0x018C  // 99 Spare

PMC_BIS3_BASE7              0x0190  // 100 base register for channel 7 DMA control
PMC_BIS3_STAT7              0x0194  // 101 Interrupt status channel 7
PMC_BIS3_WR_DMA_PNTR7       0x0198  // 102 Burst In  7
PMC_BIS3_RD_DMA_PNTR7       0x019C  // 103 Burst Out 7
PMC_BIS3_FIFORW7            0x01A0  // 104 Channel 7 DMA single write / read FIFO
PMC_BIS3_TX_AMT_LVL7        0x01A4  // 105 TX Almost Empty Count 7
PMC_BIS3_RX_AFL_LVL7        0x01A8  // 106 RX Almost Full Count 7
PMC_BIS3_TX_FIFO_COUNT7     0x01AC  // 107 TX FIFO word count 7
PMC_BIS3_RX_FIFO_COUNT7     0x01B0  // 108 RX FIFO word count 7
PMC_BIS3_FIFORW7            0x01B4  // 109 Spare
```

FIGURE 4 PMC-BISERIAL-III-LM5 XILINX ADDRESS MAP

The VendorId = 0x10EE. The CardId = 0x0027.

Register Definitions

BIS3_IO_BASE

[0x0000] Base Control Register (read/write)

Base Control Register

Data Bit	Description
31-16	Spare
15-4	Reserved
3	Master TX Enable
2	Master RX Enable
1	Force Interrupt
0	Master Interrupt Enable

FIGURE 5 PMC-BISERIAL-III-LM5 BASE CONTROL REGISTER

All bits are active high and are reset on power-up or reset command.

Master Interrupt Enable: When this bit is set to a one all enabled interrupts (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host.

Force Interrupt: When this bit is set to a one a system interrupt will occur provided the master interrupt enable is set. This is useful for interrupt testing.
Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA writes and reads respectively. The DMA interrupts are not affected by the Master Interrupt Enable.

Master TX Enable: When set '1' the channel TX start bits take effect. For independent channel operation set this bit first. For synchronized transmission set this bit last. '1' = enabled, '0' = disabled.

Master RX Enable: When set '1' the channel RX start bits take effect. For independent channel operation set this bit first. For synchronized reception enable set this bit last. '1' = enabled, '0' = disabled.

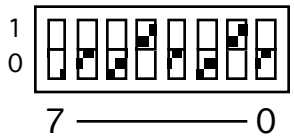
BIS3_IO_ID

[0x0004] User Switch Port (read only)

Dip-Switch Port	
Data Bit	**Description**
31-16	Spare
15-8	Xilinx Design Revision Number
7-0	Switch Setting

FIGURE 6 PMC-BISERIAL-III-LM5 USER SWITCH PORT

Switch Setting: The user switch is read through this port. The bits are read as the lowest byte. Access the read-only port as a long word and mask off the undefined bits. The dip-switch positions are defined in the silkscreen. For example the switch figure below indicates a 0x12.



Xilinx Design Revision Number: The value of the second byte of this port is the rev. number of the Xilinx design (currently 0x01 - rev. A).

BiS3_IO_STATUS

BIS3_STATUS 0x0008 // 2 base Status register

CONTROL RX

DATA BIT	DESCRIPTION
31	int_stat
30-1	Spare
0	loc_int

FIGURE 7 PMC-BISERIAL-III-LM5 INTERRUPT STATUS BIT MAP

LOC_INT = Force_int for this implementation. INT_STAT is the combination of FORCE_INT and the channel interrupts. Please also see the channel interrupts for more information.

BIS3_IO_DIR

BIS3_IO_DIR 0x000C // 3 direction register

CONTROL DIR REGISTER			
DATA BIT	**DESCRIPTION**		
31-0	DIRection	31-0	0 = read 1 = drive

FIGURE 8 PMC-BISERIAL-III-LM5 DIRECTION CONTROL BIT MAP

The direction for each of the differential pairs is controlled through this port. The port defaults to zero, which corresponds to tri-stating the drivers.

CONTROL	CORRESPONDING IO BITS
DIR_31-0	IO_31-0

Parallel termination resistors are supplied on each differential pair along with a switch to allow the user to select which lines are terminated.

The terminations for the receive groups should be set to terminate with the user software in most cases. If the Parallel Port is set to be an input with the direction bits then the corresponding termination bits should also be set.

BIS3_IO_TERM

BIS3_IO_TERM 0x001C // 7 termination register

CONTROL Term REGISTER		
DATA BIT	**DESCRIPTION**	
31-0	TERMination	31-0 1 = terminate

FIGURE 9 PMC-BISERIAL-III-LM5 TERMINATION CONTROL BIT MAP

The termination for each of the differential pairs is controlled through this port. The port defaults to zero, which corresponds to not terminating the receivers. The bits intended to be in RX mode should be programmed to terminate. Please note that channels consist of groups of 4 IO so in most cases a nibble will be set to correspond to a channel.

CONTROL	CORRESPONDING IO BIT(S)
TERM_31.0	IO_31..0

BIS3_IO_DATA

BIS3_IO_DATA 0x0010 // 4 parallel data IO DATA

Parallel Data (LVDS) IO Port	
DATA BIT	**DESCRIPTION**
31--0	parallel IO data

FIGURE 10 PMC-BISERIAL-III DATA IO BIT MAP

There are 32 potential output bits in the parallel port. The Direction and Termination register sets the direction of the bits. When the direction is set to output and the source control is set to parallel port then the bit definitions from this register are driven onto the corresponding parallel port lines.

Writing to this register puts data onto the enabled data lines [direction set].

Reading from this port returns all of the IO lines. It is possible that the output data does not match the IO data in the case of the Direction bits being set to input.

BIS3_IO_DATA_REG

BIS3_IO_DATA_REG 0x0014 // 5 parallel data register read-back

Parallel Data Register Read-back Port	
DATA BIT	**DESCRIPTION**
31-0	Data read-back from Parallel out register

FIGURE 11 PMC-BISERIAL-III DATA RDBK BIT MAP

To read the contents of the BIS3_IO_DATA port access this port. Read only. This is the direct read of the register rather than the IO signals.

BIS3_IO_MUX

BIS3_IO_MUX 0x0018 // 6 parallel data MUX control register

Parallel Port Control	
DATA BIT	**DESCRIPTION**
31-0	Parallel Port Source Definitions

FIGURE 12 PMC-BISERIAL-III PARALLEL PORT MUX CONTROL BIT MAP

Each of the Parallel Port bits has a corresponding source control bit. When the bit is set ‘1’ the parallel data is used [BIS3_IO_DATA]. When ‘0’ the defined IO is used. The LM5 design uses bits 31-0 for the 8 ports, If only a subset of the state-machine ports are used then the remaining IO can be used as a parallel port.

Please note that the direction & termination control bits need to be set to make the port bits act as inputs or outputs.

PMC_BIS3_BASE0,1,2,3,4,5,6,7

[0x0078, A0, C8, F0, 118, 140, 168, 190] Base Control Register CHANNEL(read/write)

Base Control Register

Data Bit	Description
31-8	Spare
7	RX Enable
6	TX Enable
5	Intforce : Channel Interrupt Force
4	M_INTEN : Master Channel Interrupt En
3	Read DMA Interrupt Enable
2	Write DMA Interrupt Enable
1	BYPASS : select BiPass mode
0	FFRST : FIFO Reset

FIGURE 13 PMC-BISERIAL-III-LM5 BASE CONTROL REGISTER

All bits are active high and are reset on power-up or reset command, except PLL enable, which defaults to enabled (high) on power-up or reset.

Master Interrupt Enable: When this bit is set to a one all enabled interrupts (except the DMA interrupts) will be gated through to the PCI host; when this bit is a zero, the interrupts can be used for status without interrupting the host. Applies to TX or RX State-machine interrupt depending on which is enabled.

Force Interrupt: When this bit is set to '1' a system interrupt will occur provided the master interrupt enable is set. This is useful for interrupt testing.

Write/Read DMA Interrupt Enable: These two bits, when set to one, enable the interrupts for DMA writes and reads respectively. The DMA interrupts are not affected by the Master Interrupt Enable.

TX Enable: When set to a '1', the transmitter is enabled. The transmit state-machine will begin processing data from the FIFO [assuming the Master Enable is also set] and continue until the FIFO is empty or the enable is cleared. Complete words are always sent. A transmit interrupt will be asserted when the transmit FIFO becomes empty provided the master interrupt enable is asserted.

RX Enable: When set to a '1', the receiver is enabled. The receiver will begin processing data and loading the FIFO [assuming the Master Enable is also set] and

continue until the enable is cleared. The Strobe is used to determine when to load. The last 16 clocks worth of data are loaded or whatever is in the shift register if the strobe is received with incomplete data. A receive interrupt will be asserted when the strobe is detected provided the master interrupt enable is asserted.

The FIFO should be reset after the receiver IO are defined and before the receiver is enabled to ensure that transitions caused by the IO re-definitions are not read from the FIFO.

FIFO Bypass Enable: When this bit is set to a one, any data written to the transmit FIFO will be immediately transferred to the receive FIFO. This allows for fully testing the data FIFOs without using the IO. When this bit is zero, normal operation is enabled.

PMC_BIS3_STAT0,1,2,3,4,5,6,7

[0x007C,A4, CC, F4, 11C, 144, 16C, 194] Status Read / Latch Clear Write Port

Status Register

Data Bit	Description
31	Local Interrupt Active
30-16	RX Data Count 14:0
15	Read DMA Interrupt Occurred
14	Write DMA Interrupt Occurred
13	Read DMA Error Occurred
12	Write DMA Error Occurred
11	Local Interrupt Condition Occurred
10	spare
9	RX Interrupt Occurred
8	TX Interrupt Occurred
7	Receive Data Valid
6	Receive FIFO Full
5	Receive FIFO Almost Full
4	Receive FIFO Empty
3	Spare
2	Transmit FIFO Full
1	Transmit FIFO Almost Empty
0	Transmit FIFO Empty

FIGURE 14 PMC-BISERIAL-III-LM5 STATUS PORT

Transmit FIFO Empty: When a one is read, the transmit data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Transmit FIFO Almost Empty: When a one is read, the number of data words in the transmit data FIFO is less than or equal to the value written to the PMC_BIS3_TX_AMT_LVL register; when a zero is read, the level is more than that value.

Transmit FIFO Full: When a one is read, the transmit data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive FIFO Empty: When a one is read, the receive data FIFO contains no data; when a zero is read, there is at least one data word in the FIFO.

Receive FIFO Almost Full: When a one is read, the number of data words in the receive

data FIFO is greater or equal to the value written to the PMC_BIS3_RX_AFL_LVL register; when a zero is read, the level is less than that value.

Receive FIFO Full: When a one is read, the receive data FIFO is full; when a zero is read, there is room for at least one more data word in the FIFO.

Receive Data Valid: When a one is read, there is at least one valid receive data word left. This bit can be set even if the receive FIFO is empty, because as soon as the first four words are written into the FIFO, they are read out to be ready for a PCI read DMA or single word access. When this bit is a zero, it indicates that there is no valid receive data.

RX Data Count is the sum of the RX FIFO data count plus the number of words in the pipeline. The value will be zero when no words are stored and up to the FIFO size + 4 when the FIFO is full and the pipeline is also full. The LM5 design has a 1K deep [x32] FIFO per TX or RX channel. The count can be used to determine how much data has been received when processing the RX interrupt.

TX Interrupt Occurred: When a one is read, it indicates that the transmit state-machine sent some amount of data and then the TX FIFO became empty. A zero indicates that this condition has not occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

RX Interrupt Occurred: When a one is read, it indicates that the receive state-machine has received at least one 32-bit data-word. A zero indicates that this condition has not occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Local Interrupt Condition Occurred: When a one is read, it indicates that an enabled local interrupt condition has occurred. These conditions include the TX and RX interrupts. Also the Force Interrupt bit will cause this bit to be asserted. A system interrupt will occur if the Master Interrupt Enable is set. A zero indicates that no enabled local interrupt condition is active.

Write DMA Error Occurred: When a one is read, a write DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer of one of the chaining descriptors is a one. A zero indicates that no write DMA error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Read DMA Error Occurred: When a one is read, a read DMA error has been detected. This will occur if there is a target or master abort or if the direction bit in the next pointer

of one of the chaining descriptors is a zero. A zero indicates that no read DMA error has occurred. This bit is latched and can be cleared by writing back to the Status register with a one in this bit position.

Write DMA Interrupt Occurred: When a one is read, a write DMA interrupt is latched. This indicates that the scatter-gather list for the current write DMA has completed, but the associated interrupt has yet to be completely processed. A zero indicates that no write DMA interrupt is pending.

Read DMA Interrupt Occurred: When a one is read, it indicates that a read DMA interrupt is latched. This indicates that the scatter-gather list for the current read DMA has completed, but the associated interrupt has yet to be completely processed. A zero indicates that no read DMA interrupt is pending.

Local Interrupt Active: When a one is read, it indicates that a system interrupt is asserted caused by an enabled local interrupt condition. A zero indicates that no system interrupt is pending from an enabled local interrupt condition

PMC_BIS3_WR_DMA_PNTR0,1,2,3,4,5,6,7

[0x0080, A8, D0, F8, 120, 148, 170, 198] Write DMA Pointer (write only)

DMA Pointer Address Register

Data Bit	Description
31-0	First Chaining Descriptor Physical Address

FIGURE 15 PMC-BISERIAL-III WRITE DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather write DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer containing the data to write to the device, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

PMC_BIS3_RD_DMA_PNTR0,1,2,3,4,5,6,7

[0x0084, AC, D4 FC, 124, 14C, 174, 19C] Read DMA Pointer (write only)

DMA Pointer Address Register	
Data Bit	**Description**
31-0	First Chaining Descriptor Physical Address

FIGURE 16 PMC-BISERIAL-III READ DMA POINTER REGISTER

This write-only port is used to initiate a scatter-gather read DMA. When the address of the first chaining descriptor is written to this port, the DMA engine reads three successive long words beginning at that address. The first is the address of the first memory block of the DMA buffer where the data from the device will be stored, the second is the length in bytes of that block, and the third is the address of the next chaining descriptor in the list of buffer memory blocks. This process is continued until the end-of-chain bit in one of the next pointer values read indicates that it is the last chaining descriptor in the list.

PMC_BIS3_FIFORW0,1,2,3,4,5,6,7

[0x0088, B0, D8, 100, 128, 150, 178, 1A0] Write TX/Read RX FIFO Port

RX and TX FIFO Port	
Data Bit	**Description**
31-0	FIFO data word

FIGURE 17 PMC-BISERIAL-III RX/TX FIFO PORT

This port is used to make single-word accesses to the TX and RX FIFOs.

PMC_BIS3_TX_AMT_LVL0,1,2,3,4,5,6,7

[0x008C, B4, DC, 104, 12C, 154, 17C, 1A4] TX almost-empty level (read/write)

TX Almost-Empty Level Register

Data Bit	Description
31-16	Spare
15-0	TX FIFO almost-empty level

FIGURE 18 PMC-BISERIAL-III-LM5 TX ALMOST EMPTY LEVEL REGISTER

This read/write port accesses the transmitter almost-empty level register. When the number of data words in the transmit data FIFO is equal or less than this value, the almost-empty status bit is set.

PMC_BIS3_RX_AFL_LVL0,1,2,3,4,5,6,7

[0x0090, B8, E0, 108, 130, 158, 180, 1A8] RX almost-full level (read/write)

RX Almost-Full Level Register

Data Bit	Description
31-16	Spare
15-0	RX FIFO almost-full level

FIGURE 19 PMC-BISERIAL-III RX ALMOST FULL LEVEL REGISTER

This read/write port accesses the receiver almost-full level register. When the number of data words in the receive data FIFO is equal or greater than this value, the almost-full status bit is set.

PMC_BIS3_TX_FIFO_COUNT0,1,2,3,4,5,6,7

[0x0094, BC, E4, 10C, 134, 15C, 184, 1AC] TX FIFO data count (read only)

TX FIFO Data Count Port

Data Bit	Description
31-12	Spare
11-0	TX data words stored

FIGURE 20 PMC-BISERIAL-III TX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the transmit FIFO (currently a maximum of 1K words).

PMC_BIS3_RX_FIFO_COUNT0,1,2,3,4,5,6,7

[0x0098, C0, E8, 110, 138, 160, 188, 1B0] RX FIFO data count (read only)

RX FIFO Data Count Port

Data Bit	Description
31-12	Spare
11-0	RX data words stored

FIGURE 21 PMC-BISERIAL-III RX FIFO DATA COUNT PORT

This read-only register port reports the number of 32-bit data words in the receive FIFO (currently a maximum of 1K). Please refer to the channel status register for the count including the data pipeline.

Loop-back

The Engineering kit has reference software, and includes external loop-back tests. The PMC-BiSerial-III-LM5 has a 68 pin SCSI II front panel connector. The tests transmit from channel 0->1, 2->3, 4->5, 6->7 and the reverse. An external cable with the following pins connected is required to support the tests operation.

Signal	From	To	Signal
Channel 0		Channel 1	
CLOCK+	pin 1	pin 5	CLOCK+
CLOCK+	pin 35	pin 39	CLOCK-
DATA_L+	pin 2	pin 6	DATA_L+
DATA_L-	pin 36	pin 40	DATA_L-
DATA_U+	pin 3	pin 7	DATA_U+
DATA_U-	pin 37	pin 41	DATA_U-
STROBE+	pin 4	pin 8	STROBE+
STROBE-	pin 38	pin 42	STROBE-
Channel 2		Channel 3	
CLOCK+	pin 9	pin 13	CLOCK+
CLOCK+	pin 43	pin 47	CLOCK-
DATA_L+	pin 10	pin 14	DATA_L+
DATA_L-	pin 44	pin 48	DATA_L-
DATA_U+	pin 11	pin 15	DATA_U+
DATA_U-	pin 45	pin 49	DATA_U-
STROBE+	pin 12	pin 16	STROBE+
STROBE-	pin 46	pin 50	STROBE-
Channel 4		Channel 5	
CLOCK+	pin 17	pin 21	CLOCK+
CLOCK+	pin 51	pin 55	CLOCK-
DATA_L+	pin 18	pin 22	DATA_L+
DATA_L-	pin 52	pin 56	DATA_L-
DATA_U+	pin 19	pin 23	DATA_U+
DATA_U-	pin 53	pin 57	DATA_U-
STROBE+	pin 20	pin 24	STROBE+
STROBE-	pin 54	pin 58	STROBE-
Channel 6		Channel 7	
CLOCK+	pin 25	pin 29	CLOCK+
CLOCK+	pin 59	pin 63	CLOCK-
DATA_L+	pin 26	pin 30	DATA_L+
DATA_L-	pin 60	pin 64	DATA_L-
DATA_U+	pin 27	pin 31	DATA_U+
DATA_U-	pin 61	pin 65	DATA_U-
STROBE+	pin 28	pin 32	STROBE+
STROBE-	pin 62	pin 66	STROBE-

PMC PCI Pn1 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn1 Interface on the PMC-BiSerial-III-LM5. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

TCK	-12V	1	2
GND	INTA#	3	4
		5	6
BUSMODE1#	+5V	7	8
		9	10
GND		11	12
CLK	GND	13	14
GND		15	16
	+5V	17	18
	AD31	19	20
AD28	AD27	21	22
AD25	GND	23	24
GND	C/BE3#	25	26
AD22	AD21	27	28
AD19	+5V	29	30
	AD17	31	32
FRAME#	GND	33	34
GND	IRDY#	35	36
DEVSEL#	+5V	37	38
GND	LOCK#	39	40
		41	42
PAR	GND	43	44
	AD15	45	46
AD12	AD11	47	48
AD9	+5V	49	50
GND	C/BE0#	51	52
AD6	AD5	53	54
AD4	GND	55	56
	AD3	57	58
AD2	AD1	59	60
	+5V	61	62
GND		63	64

FIGURE 22 PMC-BISERIAL-III-LM5 PN1 INTERFACE

PMC PCI Pn2 Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module PCI Pn2 Interface on the PMC-BiSerial-III-LM5. See the User Manual for your carrier board for more information. Unused pins may be assigned by the specification and not needed by this design.

+12V		1	2
TMS	TDO	3	4
TDI	GND	5	6
GND		7	8
		9	10
		11	12
RST#	BUSMODE3#	13	14
	BUSMODE4#	15	16
	GND	17	18
AD30	AD29	19	20
GND	AD26	21	22
AD24		23	24
IDSEL	AD23	25	26
	AD20	27	28
AD18		29	30
AD16	C/BE2#	31	32
GND		33	34
TRDY#		35	36
GND	STOP#	37	38
PERR#	GND	39	40
	SERR#	41	42
C/BE1#	GND	43	44
AD14	AD13	45	46
GND	AD10	47	48
AD8		49	50
AD7		51	52
		53	54
	GND	55	56
		57	58
GND		59	60
		61	62
GND		63	64

FIGURE 23 PMC-BISERIAL-III-LM5 PN2 INTERFACE

BiSerial III Front Panel IO Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface on the PMC BiSerial-III-LM5. Also, see the User Manual for your carrier board for more information. For customized versions, or other options, contact Dynamic Engineering.

IO_0p CLK0+	IO_0m CLK0-	1	35
IO_1p DAT0_L+	IO_1m DAT0_L-	2	36
IO_2p DAT0_U+	IO_2m DAT0_U-	3	37
IO_3p STB0+	IO_3m STB0-	4	38
IO_4p CLK1+	IO_4m CLK1-	5	39
IO_5p DAT1_L+	IO_5m DAT1_L-	6	40
IO_6p DAT1_U+	IO_6m DAT1_U-	7	41
IO_7p STB1+	IO_7m STB1-	8	42
IO_8p CLK2+	IO_8m CLK2-	9	43
IO_9p DAT2_L+	IO_9m DAT2_L-	10	44
IO_10P DAT2_U+	IO_10m DAT2_U-	11	45
IO_11P STB2+	IO_11m STB2-	12	46
IO_12p CLK3+	IO_12m CLK3-	13	47
IO_13p DAT3_L+	IO_13m DAT3_L-	14	48
IO_14p DAT3_U+	IO_14m DAT3_U-	15	49
IO_15p STB3+	IO_15m STB3-	16	50
IO_16p CLK4+	IO_16m CLK4-	17	51
IO_17p DAT4_L+	IO_17m DAT4_L-	18	52
IO_18p DAT4_U+	IO_18m DAT4_U-	19	53
IO_19p STB4+	IO_19m STB4-	20	54
IO_20p CLK5+	IO_20m CLK5-	21	55
IO_21p DAT5_L+	IO_21m DAT5_L-	22	56
IO_22p DAT5_U+	IO_22m DAT5_U-	23	57
IO_23p STB5+	IO_23m STB5-	24	58
IO_24p CLK6+	IO_24m CLK6-	25	59
IO_25p DAT6_L+	IO_25m DAT6_L-	26	60
IO_26p DAT6_U+	IO_26m DAT6_U-	27	61
IO_27p STB6+	IO_27m STB6-	28	62
IO_28p CLK7+	IO_28m CLK7-	29	63
IO_29p DAT7_L+	IO_29m DAT7_L-	30	64
IO_30p DAT7_U+	IO_30m DAT7_U-	31	65
IO_31p STB7+	IO_31m STB7-	32	66
IO_32p	IO_32m	33	67
IO_33p	IO_33m	34	68

FIGURE 24 PMC-BISERIAL-III-LM5 FRONT PANEL INTERFACE

Pn4 IO is available as a customer option. The Pn4 IO are isolated on the LM5 base version. For rear panel IO options please contact Dynamic Engineering.

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

ESD
Proper ESD handling procedures must be followed when handling the PMC-BiSerial-III-LM5. The card is shipped in an anti-static, shielded bag. The card should remain in the bag until ready for use. When installing the card the installer must be properly grounded and the hardware should be on an anti-static workstation.

Start-up
Make sure that the "system" can see your hardware before trying to access it. Many BIOS will display the PCI devices found at boot up on a "splash screen" with the VendorID and CardId and an interrupt level. If the information is not available from the BIOS then a third party PCI device cataloging tool will be helpful. PCIView is an example.

Watch the system grounds
All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

We provide the components. You provide the system. Only careful planning and practice can achieve safety and reliability. Inputs can be damaged by static discharge, or by applying voltage outside of the device rated voltages.

Construction and Reliability

PMC Modules were conceived and engineered for rugged industrial environments. The PMC-BiSerial-III-LM5 is constructed out of 0.062-inch thick ROHS compliant material.

Through-hole and surface-mount components are used. The PMC connectors are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC is secured against the carrier with four screws attached to the 2 stand-offs and 2 locations on the front panel. The four screws provide significant protection against shock, vibration, and incomplete insertion.

The PMC Module provides a low temperature coefficient of 2.17 W/°C for uniform heat. This is based upon the temperature coefficient of the base material of 0.31 W/m-°C, and taking into account the thickness and area of the PMC. The coefficient means that if 2.17 Watts are applied uniformly on the component side, then the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The PMC-BiSerial-III-LM5 design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one Watt is required to be dissipated due to external loading, then forced-air cooling is recommended. With the one degree differential temperature to the solder side of the board, external cooling is easily accomplished.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.
http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
Dynamic Engineering
435 Park Dr.
Ben Lomond, CA 95005
831-336-8891
831-336-3840 fax
support@dyneng.com

Specifications

Host Interface:	[PMC] PCI Mezzanine Card – 32-bit, 33 MHz
Serial Interfaces:	8 serial interfaces programmable In or Out. 32-bit word size, MSB first, 2 bits parallel, multiple words, reference clock, Strobe. Data changes on the falling edge and valid on the rising edge of the channel clock.
TX Bit-rates generated:	40 MHz is the standard TX rate. Internal reference at 66 MHz on IO side of FIFO's means alternate frequency up to 60 MHz can be accommodated with an Osc. Change. PLL available but not implemented in this design.
Software Interface:	Control Registers, FIFOs, and Status Ports
Initialization:	Hardware reset forces all registers to 0 except as noted
Access Modes:	LW boundary Space (see memory map)
Wait States:	One for all addresses
Interrupt:	TX done, RX data received, read, and write DMA done
DMA:	Scatter/Gather DMA Support implemented
Onboard Options:	All Options are Software Programmable
Interface Options:	68 pin twisted pair cable 68 screw terminal block interface
Dimensions:	Standard Single PMC Module
Construction:	ROHS compliant FR-370HR Multi-Layer Printed Circuit, Through-Hole and Surface-Mount Components. ROHS or leaded builds are available.
Temperature Coefficient:	2.17 W/^{o}C for uniform heat across PMC
Power:	Max. **TBD** mA @ 5V
Temperature range	Standard (0 to +70) Extended Temperature available (-40 to +85)

Order Information

PMC-BiSerial-III-LM5	PMC Module with 8 half duplex serial channels, LVDS IO, 32-bit data interface. 2 bit serial at 40 MHz for 80 Mbits/sec standard transfer rate. DMA support.
Eng Kit PMC-BiSerial-III-LM5	HDEterm68 - 68 position screw terminal adapter http://www.dyneng.com/HDEterm68.html HDEcabl68 - 68 IO twisted pair cable http://www.dyneng.com/HDEcabl68.html Technical Documentation, 1. PMC-BiSerial-III Schematic 2. PMC-BiSerial-III-LM5 Driver software and user application. Data sheet reprints are available from the manufacturer's web site

***Note**: The Engineering Kit is strongly recommended for first time* PMC BiSerial-III *purchases.*

Schematics

Schematics are provided as part of the engineering kit for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.